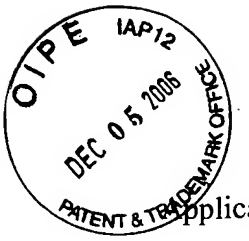
Express Mail No.: EV829959475US
GE-120432
PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: David Collier et al.

Art Unit: 2157

Serial No.: 10/056,596

Examiner: Gold, Avi M

Filed: January 24, 2002

For: METHODS AND SYSTEMS FOR MANAGEMENT AND CONTROL OF AN AUTOMATION CONTROL MODULE

DECLARATION OF CONCEPTION OF PRIOR INVENTION (37 C.F.R. § 1.131)

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

David Collier, whose address is 1626 Farm Brook Pl., Charlottesville, VA 22901,

Ferrell Mercer, whose address is 4940 Summer Lane, Earlysville, VA 22936,

Bill Hannold, whose address is 4645 Spotswood Trail, Barboursville, VA 22923,

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Dave Hietanen, whose address is 3500 Springfield Road, Charlottesville, VA 22911,

Robert Chambers, whose address is 2904 SW Silverspur Rd, Lees Summit, VA 64081, and

David Elliott, whose address is 1595 Merriefields Lane, Ruckersville, VA 22968, declare as follows:

1. This declaration is to establish an actual reduction to practice of the invention claimed in the above-referenced application at a date prior to September 21, 2001.

2. We have reviewed and understand the patent application referenced in the caption above (hereafter "Subject Application"), including the specification, abstract, drawings and claims therefor.

3. We have reviewed United States Patent No. 6,725,104 B2 titled "Method and Apparatus for E-Mail Based Communication with Automated Facilities and Devices" filed on September 21, 2001, and issued April 20, 2004, which, on information and belief, is being relied on in at least one rejection of the claims of the Subject Application (hereafter "Antedated Reference").

4. We are the inventors of the invention(s) recited in the claims of the Subject Application (hereafter "Claimed Invention").

5. The Claimed Invention of the Subject Application was conceived and actually reduced to practice before September 21, 2001, which is the effective filing date of the Antedated Reference.

6. The Claimed Invention was actually reduced to practice in the United States.

7. As evidence that the Claimed Invention of the Subject Application was actually reduced to practice before the effective filing date of the Antedated Reference, attached is a true and accurate copy of a screen shot showing time line information for assembly of an E35A1 Board in connection with the Subject Application (see Appendix A).

8. As seen in Appendix A, an assembly of the E35A1 Board was received by a Design Engineer prior to the Antedated Reference effective date of September 21, 2001.

9. As evidence that the Claimed Invention of the Subject Application was actually reduced to practice before the effective filing date of the Antedated Reference, attached is a true and accurate copy of a screen shot showing ordering information for a Working Model of E35A1 in connection with the Subject Application (see Appendix B).

10. As seen in Appendix B, a Working Model of an E35A1 Board, described as "Embedded 10/100 Ethernet...," was requested to be fabricated before the effective filing date of the Antedated Reference.

11. As further evidence that the Claimed Invention of the Subject Application was actually reduced to practice before the effective filing date of the Antedated Reference, attached is a true and accurate copy of a board hardware description (hereafter "Board Description") that was prepared in connection with the Subject Application (see Appendix C) The Board Description includes, on sheet 5, a description of a new board, which is a 90-30 10/100base-T Embedded Ethernet Controller CPU product and the Board Description also includes figure 4-1, which illustrates an E35A1 Daughterboard w/Serial Port & 10/100base-T Ethernet. As described on sheet 5 of the Board Description, the 90-30 10/100base-T Embedded Ethernet Controller CPU product is a part of a CPU 374 module.

12. As further evidence that the Claimed Invention of the Subject Application was actually reduced to practice before the effective filing date of the Antedated Reference, attached

is a true and accurate copy of an user interaction specification (hereafter "User Specification") that was prepared in connection with the Subject Application (see Appendix D).

13. The User Specification is titled "90-30 CPU374/Web Server User Interaction Specification" and includes thirty-one (31) pages of statements and drawings describing and illustrating the invention.

14. The User Specification was authored by co-inventor Dave Collier.

15. As illustrated in Figure 1 and on pages 3-4 of the User Specification, a web page informs a user to consult their user documentation or contact their vendor for instructions on how to transfer web pages to the PLC via FTP that will enable viewing of PLC data. Moreover, as illustrated on page 5 of the User Specification, each browser instance requires one TCP connection and each FTP session requires two TCP connections to the PLC.

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We hereby declare that all statements made herein of my own knowledge are true and that all statements made on Information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

David S. Collier 11/14/06
David Collier (Date)

Ferrell Mercer 11/14/2006
Ferrell Mercer (Date)

Bill Hannold 11/14/06
Bill Hannold (Date)

Jason Kadingo (Date)

Bob Newman 11/15/06
Bob Newman (Date)

Brad Bolfing 11/19/06
Brad Bolfing (Date)

Dave Hietanen (Date)

11/14/06
Carrie Brownhill (Date)

Robert Chambers (Date)

11/14/06
David Elliott (Date)

We hereby declare that all statements made herein of my own knowledge are true and that all statements made on Information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

David Collier	(Date)	Ferrell Mercer	(Date)
Bill Hannold	(Date)	Jason Kadingo	(Date)
Bob Newman	(Date)	Brad Bolfing	(Date)
Dave Hietanen	11/21/06 (Date)	Carrie Brownhill	(Date)
Robert Chambers	(Date)	David Elliot	(Date)

We hereby declare that all statements made herein of my own knowledge are true and that all statements made on Information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

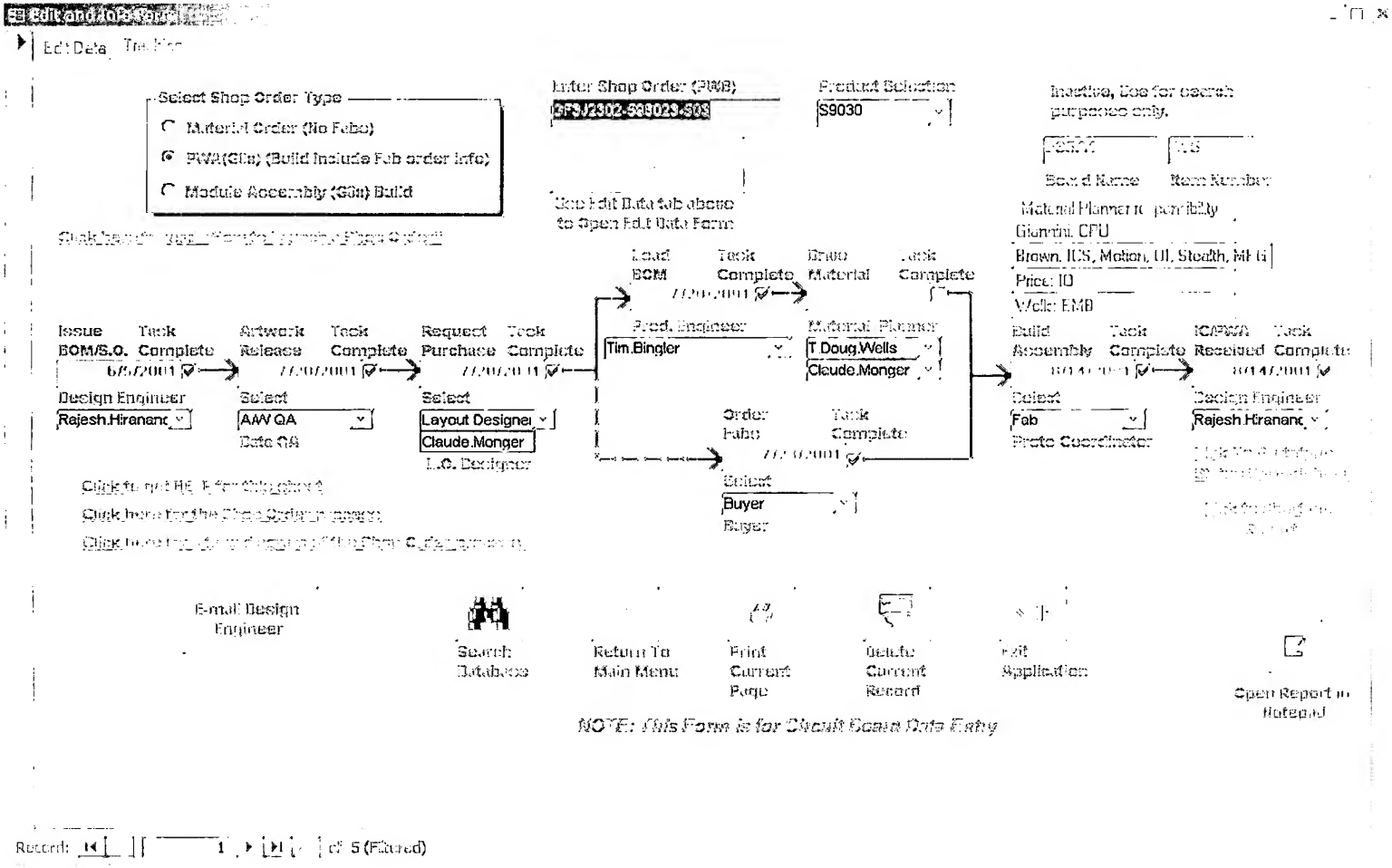
David Collier	(Date)	Ferrell Mercer	(Date)
Bill Hannold	(Date)	Jason Kadingo	(Date)
Bob Newman	(Date)	Brad Bolfing	(Date)
Dave Hietanen	(Date)	Carrie Brownhill	(Date)
Robert Chambers	11/16/06 (Date)	David Elliott	(Date)

GE-120432
PATENT

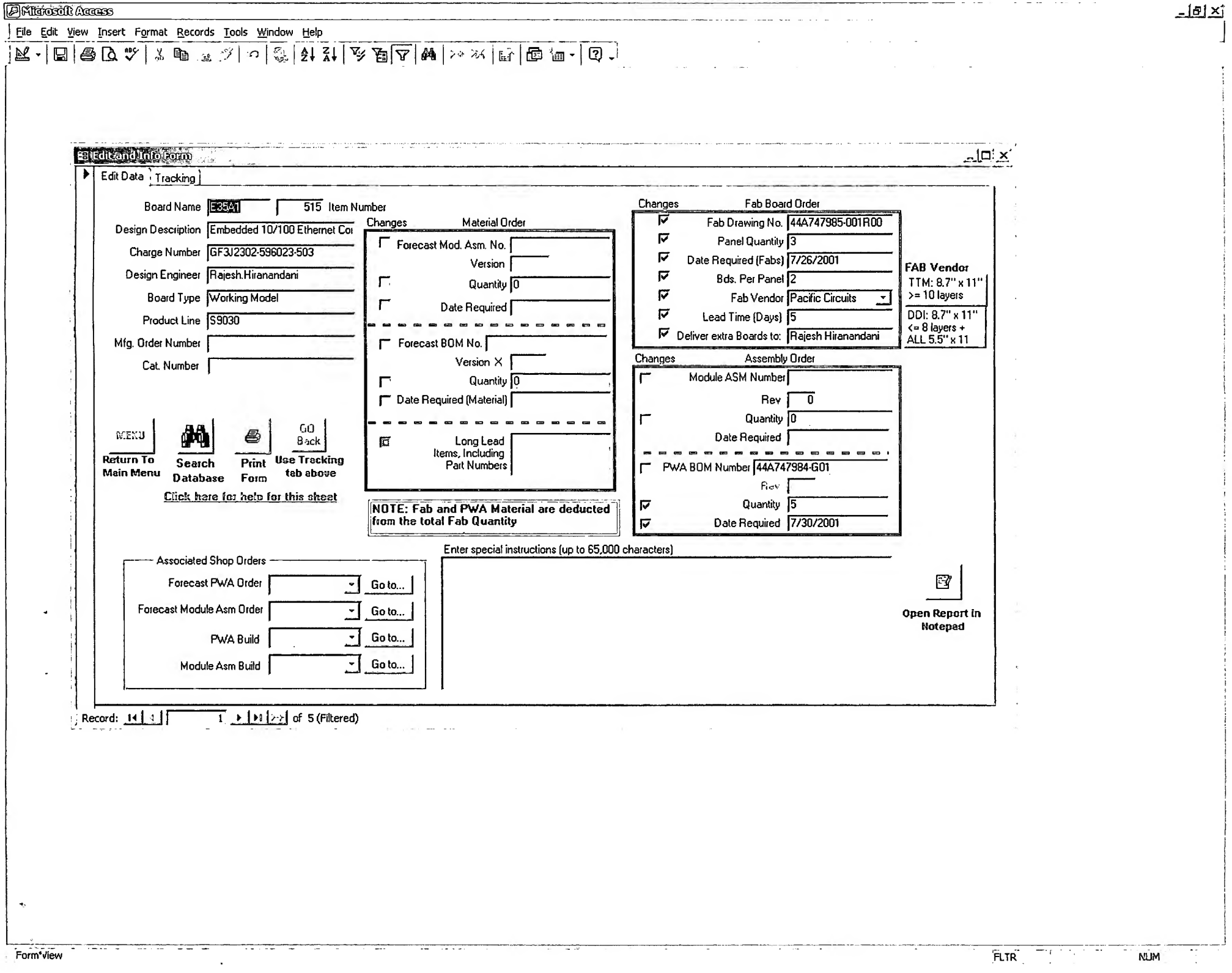
We hereby declare that all statements made herein of my own knowledge are true and that all statements made on Information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

David Collier	(Date)	Ferrell Mercer	(Date)
Bill Hannold	(Date)	Jason Kadingo 11/22/2006	(Date)
Bob Newman	(Date)	Brad Bolfing	(Date)
Dave Hietanen	(Date)	Carrie Brownhill	(Date)
Robert Chambers	(Date)	David Elliott	(Date)

APPENDIX A


File Edit View Insert Format Records Tools Window Help
Edit Data
Select Shop Order Type
Material Order (No Febo)
PWA(Glbs) (Build Include Fab order info)
Module Assembly (Glbs) Build
Enter Shop Order (PWB)
SFSJ2302-S89023-S03
Product Selection
S9030
Inactive, Use for search purposes only.
Board Name
Item Number
Use Edit Data tab above to Open Edit Data Form
Material Planner responsibility
Glenn.in, CFU
Brown, ICS, Motion, UI, Stealth, MFG
Price: IO
Wells: EMB
Load BOM
Task Complete
Bring Material
Task Complete
Issue BOM/S.O.
Task Complete
Artwork Release
Task Complete
Request Purchase
Task Complete
Prod. Engineer
Tim.Bingler
Material Planner
T.Doug.Wells
Claude.Monger
Build Assembly
Task Complete
ICA/PWA Received
Task Complete
Design Engineer
Rajesh.Hiranand
Select
AAV QA
Date QA
Select
Layout Designe
Claude.Monger
L.O. Designer
Order Febo
Task Complete
Select
Buyer
Buyer
Select
Fab
Febo Coordinator
Design Engineer
Rajesh.Hiranand
E-mail Design Engineer
Search Database
Return To Main Menu
Print Current Page
Delete Current Record
Exit Application
Open Report in Notepad
NOTE: This Form is for Circuit Board Data Entry
Record: 1 of 5 (Filtered)
Form View

APPENDIX B


Microsoft Access
File Edit View Insert Format Records Tools Window Help
Edit and Info Form
Edit Data
Tracking
Board Name
E35A1
515
Item Number
Design Description
Embedded 10/100 Ethernet Co
Charge Number
GF3J2302-596023-503
Design Engineer
Rajesh.Hiranandani
Board Type
Working Model
Product Line
S9030
Mfg. Order Number
Cat. Number
MENU
Return To Main Menu
Search Database
Print Form
GO Back
Use Tracking tab above
Click here for help for this sheet
Changes
Material Order
Forecast Mod. Asm. No.
Version
Quantity
0
Date Required
Forecast BOM No.
Version X
Quantity
0
Date Required (Material)
Long Lead Items, Including Part Numbers
NOTE: Fab and PWA Material are deducted from the total Fab Quantity
Changes
Fab Board Order
Fab Drawing No.
44A747985-001R00
Panel Quantity
3
Date Required (Fabs)
7/26/2001
Bds. Per Panel
2
Fab Vendor
Pacific Circuits
Lead Time (Days)
5
Deliver extra Boards to:
Rajesh Hiranandani
FAB Vendor
TTM: 8.7" x 11" >= 10 layers
DDI: 8.7" x 11" <= 8 layers + ALL 5.5" x 11
Changes
Assembly Order
Module ASM Number
Rev
0
Quantity
0
Date Required
PWA BOM Number
44A747984-G01
Rev
Quantity
5
Date Required
7/30/2001
Associated Shop Orders
Forecast PWA Order
Go to...
Forecast Module Asm Order
Go to...
PWA Build
Go to...
Module Asm Build
Go to...
Enter special instructions (up to 65,000 characters)
Open Report in Notepad
Record:
1
of 5 (Filtered)
Form View
FLTR
NUM

APPENDIX D

TITLE

90-30 CPU374/Web Server
User Interaction Specification

DISTRIBUTION:

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	DATE	NAME	VERSION 1.01	
Author	[redacted]	Dave Collier	**DOCUMENT STATUS**	GE Fanuc Automation Charlottesville, Virginia USA
Team Lead	[redacted]	Carrie Brownhill	Released	
Manager	[redacted]	Bill Huntley	**UIS-20001113- DSC-1**	PAGES 31

Revisions

Version	Date	Page-paragraph	Remarks
0.01	[redacted]		Initial draft.
0.02	[redacted]		Updates from review on [redacted]
0.03	[redacted]		Updates from review closed on [redacted]
1.00	[redacted]		Updates from review on 0.03
1.01	[redacted]	Section 2.2 p.4	Change superuser to user to avoid confusion with station manager superuser intended for only GE Fanuc use per D. Hietanen's request

List Of Figures

1. Introduction

This document specifies the user interface to the web pages served by the 90-30 CPU374 web server.

1.1. Scope

This document applies only to the Web server component of the CPU374. The web server user interface includes the following web pages:

1. CPU374 PLC Status Viewer Page
2. Reference Table Viewer Page
3. PLC Fault Table Viewer Page
4. I/O Fault Table Viewer Page

1.2. Applicable Documents

1. *CPU374 System User Interaction Specification,* UIS_20000830_BJB_1, Brad Bolfing, version 1.00, [redacted].
2. *CPU374 System Requirements Document,* SRD_20000412_BJB_1, Brad Bolfing, version 1.00, [redacted].
3. *VersaMax CPUE05/Ethernet User Interaction Specification,* UIS_WWT-1-073099, version 1.10, [redacted].
4. *Logicmaster 90-30/20/Micro Programming Software User's Manual –* [redacted]*8 GFK-0466L.*

1.3. Document Location and Links

Name and location of this document:

PC Access: \\chopdsrv2\shared\90-30\Data\cpu374\E35A1 10-100 Ethernet Daughterboard\Interface Documents\enet_user_interface\cpu374_webserver_uis_100.doc

UNIX Access: None

A prototype of the web pages in this document is available at the following location:

\\chopdsrv2\shared\90-30\Data\cpu374\E35A1 10-100 Ethernet Daughterboard\WebEnabling\Webpages\working dsc\cpu374_8\index.htm

Note: this prototype is provided to give an idea of the look and feel of the user interface. Not all functions are implemented or working as specified in this document. The prototype should be used with Internet Explorer.

1.4. Definition of Terms

CGI

The Common Gateway Interface (CGI) is a standard for interfacing external applications with information servers, such as HTTP or Web servers. A plain HTML document that the Web server **retrieves** is **static**, which means it exists in a constant state: a text file that doesn't change. A CGI program, on the other hand, is **executed** in real-time, so that it can output **dynamic** information. For example, you want to "hook up" your Unix database to the World Wide Web to allow people from all over the world to query it. In this case you would create a CGI program that the Web server will execute to transmit information to the database engine, and receive the results back again and display them to the client. This is an example of a *gateway*, and this is where CGI, currently version 1.1, got its origins.

JavaScript

Interpreted programming language embedded in a Web page's HTML to allow more dynamic web pages including programs that interact with the user, control the browser and dynamically create HTML content. Javascript programs are executed by the browser.

URL

A web browser uses a Uniform Resource Locator (URL) to access specific web pages and other items on a web server (for example http://www.servername.com/web-server.htm). It consists of three parts: 1) The protocol ("http") , 2) the server name ("www.servername.com") and 3) The file name ("web-server.htm"). For example to access a static web page, the browser connects to the server machine by using a name server to translate the server name into an IP address and then uses an http protocol GET request to load the specified file.

2. Specification

This chapter describes the user interactions with the Web pages served by the CPU374 Web server and is intended to meet the requirements specified in the *CPU374 System Requirements Document,* SRD_20000412_BJB_1, Brad Bolfing, version 1.00, [redacted] described in section 4.30 (Web Enable the CPU374).

2.1. General SRD Requirements

All of the following web pages will be designed to meet the following general web enabling SRD requirements (note: the numbers given below follow the same numbering used in the SRD):

5. The Browser (client) and PLC (server) interface shall be designed to facilitate the transfer of PLC data through local web firewalls.
6. This functionality shall be compatible with Netscape and Internet Explorer Browsers.
7. The Browser host operating systems that will be supported are Windows NT, Windows 95, Windows 98, and Windows 2000, and Windows Millenium.
8. Since the anticipated design calls for use of Java, the version of the Browser shall be capable of running the Java Virtual Machine (JVM) version 1.3 plug-in.

The other SRD requirements are listed with the section that meets that requirement.

2.2. General Specifications

The CPU374 web server will ship with the following default web page (index.htm) which will be shown after entering the PLC's URL or IP address in the location or address box or the user's browser.

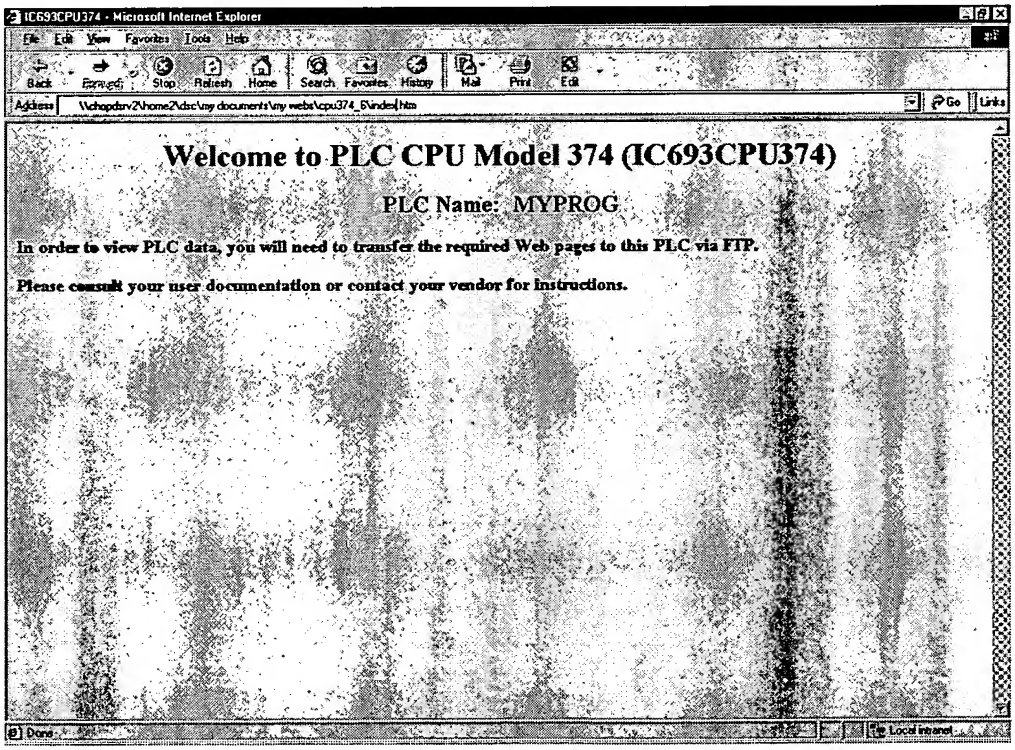

Figure 1 – Default CPU374 Web Page

For the final product the translated versions of the English text on this page will also be shown on the same page in the following languages: French, German and Spanish. This page informs the user to consult their user documentation or contact

their vendor for instructions on how to transfer web pages to the PLC via FTP that will enable viewing of PLC data. This approach allows GE Fanuc to supply the correct web pages based on the customer profile (selling company and language). Location and delivery of the web pages will be determined by the marketing organization before release of the product. Possible sources include a diskette shipped with the product or download from a web site.

Once the customer has determined the location of the required web pages, the user will need to ftp the specified files to the PLC. The user can either use a ftp tool or use the "ftp" command on the DOS Prompt or Command line (Note: not all ftp tools will be guaranteed to work since the server only supports a limited set of ftp commands). Using the Command line entry, the user will enter "ftp" followed by the URL or IP address of the PLC as shown below:

ftp <URL or ip address of board>

The user will then be prompted for a login name and password as shown below:

login: <anonymous or user>
password: ???

The user has a choice of logging in as "anonymous" or "user". If "anonymous" is entered at the login prompt, the user will be asked for a password which must match the ftp anonymous password stored in the PLC. If the login is successful, the user will have read-only privileges and can successfully execute the "binary", "get", "ls", "dir", "quit" and "bye" commands listed below.

If "user" is entered at the login prompt, the user will be asked for a password which must match the ftp user password stored in the PLC. Once successfully logged on, the user can execute any of the ftp commands described below. This type of login is required in order to store new web pages to the server.

The default anonymous and user passwords will be blank "". The user can change the anonymous and user ftp passwords through a parameter in the AUP file, which is stored to the PLC via the programmer, or through the station manager. The following line or lines should be added to the AUP file to change the anonymous and user ftp passwords respectively:

user_ftp_password = my_user_pw

anon_ftp_password = my_an_pw

In addition, the user can change the user and anonymous ftp passwords (for example to "my_su_pw" and "my_an_pw") using the following station manager commands respectively:

CHPARM user_ftp_password my_user_pw

CHPARM anon_ftp_password my_an_pw

Both passwords can be up to 10 characters long and accept the same character set listed for the reference viewer password described later in this document. The passwords are case insensitive.

Arguments for Station Manager CHPARM commands must be enclosed in double quotes to preserve the capitalization of the argument. However since these passwords are case insensitive, the double quotes are not required.

Note: the CHPARM commands are not available if the PLC has received a valid configuration from the programmer.

After logging into the PLC's ftp server as a user, web pages can be copied to the PLC through the following steps:

1. Set the file transfer type to binary by typing in "binary"
2. Transfer each file using one "put" command per file by typing in: "put filename1.htm"
3. Verify all files are properly transferred by typing in: "dir" or "ls". This will return a list of the files located on the web server. The web server directory consists of a single level with no subdirectories. At a minimum, the server will return the file name, the date and time and the size of the files.
4. Quit the ftp session by typing in "quit" or "bye".

If the user copies a file that already exists in the module, the new file will overwrite the existing file without warning the user. One of the files stored will be a fault string file that will be specific for each language supported (see the Internationalization section for more details).

The ftp server will also support the following other commands:

1. "get" command - allows the user to transfer files from the PLC web server to their local PC (for example "get filename1.htm").
2. "delete" command – allows user to delete web pages from the server (for example "delete filename1.htm").

After storing the required web pages to the module, the user must enter the full URL in the Address or Location box in the browser window. If the user does not enter a file name after the URL, the web server will default to using the index.htm file. The user can also directly access the following web pages on the server:

1. URL\index.htm: This is the PLC status page.
2. URL\reference_tables.htm: This is the reference table viewer page.
3. URL\PLC_fault_tables.htm: This is the PLC fault table viewer page.
4. URL\IO_fault_tables.htm: This is the I/O fault table viewer page.

The user must be using Version 4.0 or greater of either Netscape Navigator or Internet Explorer. Since there are some differences in the way different web browsers display pages, the look of the web page will be optimized for best presentation with Internet Explorer. In addition, the browser must be capable of running the Java Virtual Machine (JVM) version 1.3 plug-in case Java applets are required for implementation. The supported browser host operating systems are Windows NT 4.0 SP5 or SP6, Windows 95B, Windows 98 (First Edition Service Pack 1, Second Edition), and Windows 2000 Professional SP1, and Windows Millenium Edition. In order to see the entire PLC Status and Reference Table pages, the user will need to set their screen resolution for 1024 x 768 or higher. Local web firewall blocking issues will be avoided by using HTTP protocol on port 80 to transfer standard HTML files including JavaScript and Java applets from the server to the browser and HTTP Post command to transfer form information from the browser to the server.

Each browser instance requires one TCP connection and each FTP session requires two TCP connections to the PLC. The number of browsers or ftp connections to the PLC at any one time is configurable from 0 to 12 with 0 meaning the web server capability is disabled. Once the number of browser/ftp connections reaches the configurable limit, any new browser or ftp connection requests will fail. The number of http/ftp connections is configurable via the programmer. The programmer configuration details are described in the*CPU374 System User Interaction Specification,* UIS_20000830_BJB_1, Brad Bolfing, version 1.00, [redacted].. The default value for this parameter will be 2.

In addition, the user can change the number of http/ftp connections with the following station manager command:

CHPARM http_ftp_connections <number from 0-12>

For example:

CHPARM http_ftp_connections 6

Note: the CHPARM commands are not available if the PLC has received a valid configuration from the programmer.

2.3. CPU374 PLC Status Viewer Page

2.3.1. SRD Requirements

This web page meets the following SRD requirements described in section 4.30.2.

3. Reading and Display of PLC Status Information including Memory and Reference Information shall be supported.

2.3.2. Description

The CPU374 PLC Status Viewer Page provides an entry point into the web server. Once the proper address is supplied the PLC Status Viewer page will appear as shown below:

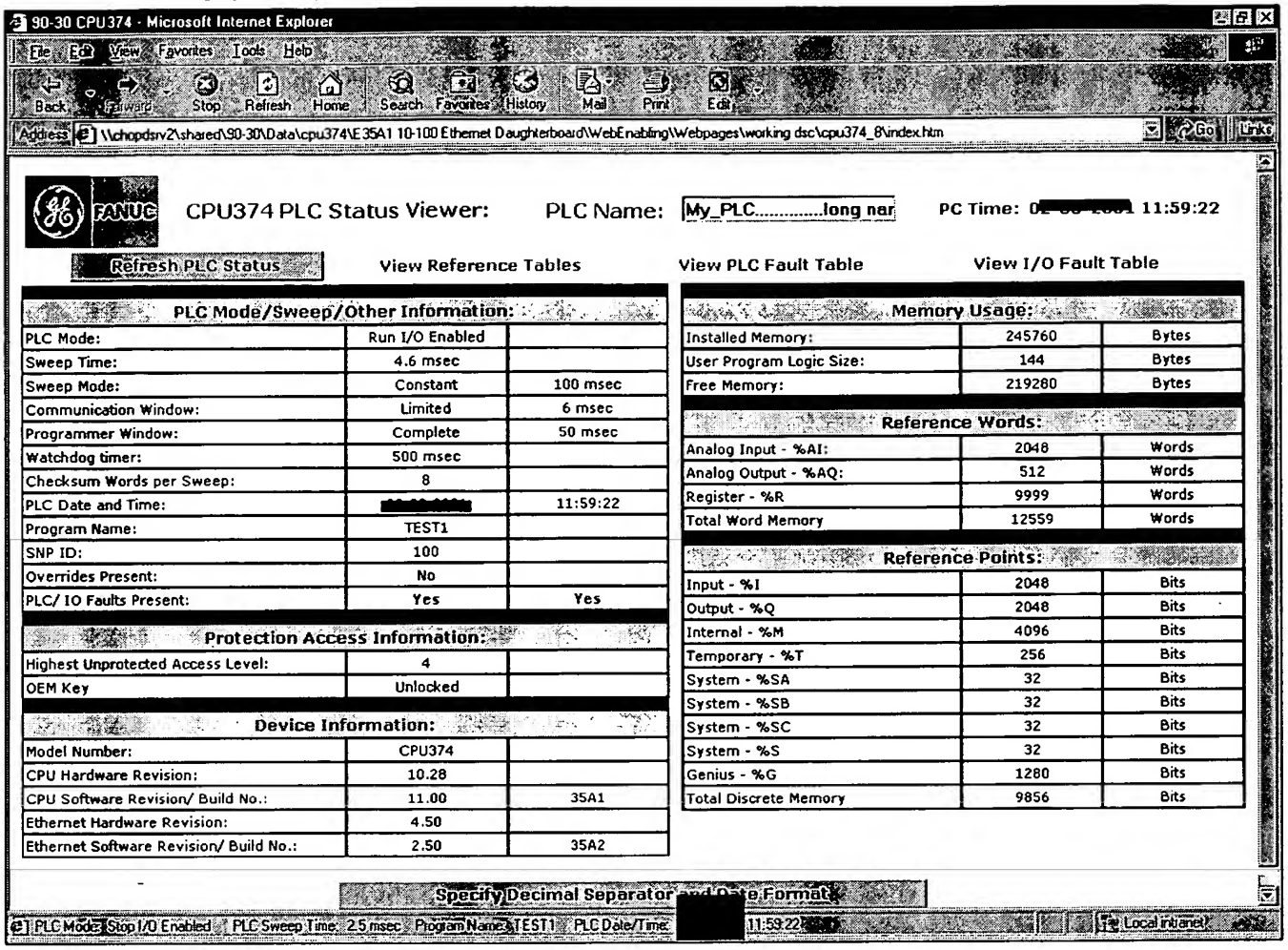

Figure 2- PLC Status Viewer Page

From this initial screen, the user can view PLC status and also navigate to the other CPU374 web pages (Reference Tables Viewer, PLC Fault Table and I/O Fault Table). In addition, the PC date and time is shown in the upper right hand corner. This represents the PC's date and time when the page was loaded by the browser. Also, the GE Fanuc logo in the upper left-hand corner will be clickable and linked to www.gefanuc.com. The following PLC status information will be provided on this screen:

1. PLC Name: In the textbox at the top of the screen, the first 15 characters of the PLC name will be displayed. The PLC name can contain any standard character (alphanumeric characters and the following other characters: ! @ # $ % ^ & * ( ) _ - + = { } | [ ] \ ~ ` : " ; ' < > ? , . /) with a length of 1 to 64 characters. For names longer than 15 characters, the user can select the textbox and scroll to the rest of the name. In addition, the user can select the name and paste it to another application to see the entire name in a single view. The default PLC name will be the PLC program name.

   The user may change the PLC name by adding the following line in the AUP file stored to the PLC:

   enet_plc_name = "My_PLC"

   In addition, the user can change the PLC name (for example to "My_PLC") using the following station manager command:

CHPARM enet_plc_name "My_PLC"

The PLC name must be enclosed in double quotes to preserve the capitalization. If double quotes are not used, the text is converted to lower case.

Note: the CHPARM commands are not available if the PLC has received a valid configuration from the programmer.

The PLC name cannot be changed through the web server interface. If the user changes the text in the textbox directly, the text in the textbox will change back to the name stored in the PLC when the cursor leaves the textbox.

2. PLC Mode/Sweep/Other information:
   a. PLC Mode: Run I/O Enabled, Stop I/O Enabled, Stop I/O Disabled or Stop Faulted.
   b. Sweep time: given in milliseconds to the closest 0.1 millisecond.
   c. Sweep Mode – Normal or Constant. If "Constant" is displayed, the constant sweep time should also be displayed in the right column and the Communication Window and Programmer Window should be marked as "N/A". If "Normal" is displayed, the cell in the third column is blank.
   d. Communication Window – Complete, Limited or NA if "Constant" Sweep Mode is displayed. The third column shows "6 msec" when "Limited" is displayed and "50 msec" when "Complete" is displayed.
   e. Programmer Window - Complete, Limited or NA if "Constant" Sweep Mode is displayed. The third column shows "6 msec" when "Limited" is displayed and "50 msec" when "Complete" is displayed.
   f. Watchdog timer – time in milliseconds.
   g. Checksum Words per sweep –the number of user program words added to the running user program checksum per sweep.
   h. PLC Date & Time: the PLC date and time when the web page was requested (for example, [redacted] – 13:51:16)
   i. Program Name: the name of the current user program stored to the PLC. This is referred to as the folder name in Logicmaster and VersaPro.
   j. SNP ID: 7 character ID to uniquely identify the PLC on a multi-drop serial bus.
   k. Overrides Present: this will show "Yes" if any of the discrete bits in the %I, %Q, %M, or %G tables are overridden otherwise it will show "No". This is based on %S0011 (1 = Yes, 0 = No) which is programmer alias OVR_PRE.
   l. PLC/ IO Faults Present: The value in the first and second columns will represent the status of the PLC and I/O Fault tables respectively. If there are any faults in the respective table, the value will be "Yes" otherwise the value will be "No". The value will contain a hyperlink to the respective table so that by clicking on the value for the PLC fault table, the user will be taken to the PLC Fault Table. The values for these entries will be determined by the status of the following %S bits: %SC0012 (1 = Yes, 0 = No) for the PLC Fault table programmer alias SY_PRES and %SC0013 (1= Yes, 0 = No) for the I/O Fault Table programmer alias IO_PRES.
3. Protection Access Information:
   a. Access Level - the highest unprotected level (4, 3 or 2).
   b. OEM Key – locked or unlocked state.
4. Device Information
   a. Model Number: CPU374.
   b. CPU Hardware Revision: revision of the CPU hardware.
   c. CPU Software Revision/ Build Number: CPU firmware revision and build number.
   d. Ethernet Hardware Revision: revision of the Ethernet hardware.
   e. Ethernet Software Revision/ Build Number: Ethernet firmware revision and build number.

5. Memory Usage:
   a. Installed Memory: the memory capacity of the CPU374 in bytes.
   b. Program Logic size: the program logic size in bytes.
   c. Free memory: the amount of memory in bytes available for both logic and configuration.
6. Reference Words: displays the sizes of the each of the following word tables. These values are configurable by the user through the programmer hardware configuration software package.
   a. Analog Input – the number of analog input registers currently available.
   b. Analog Output – the number of analog output registers currently available.
   c. Register – the number of general registers currently available.
   d. Total Word Memory – Total word memory currently available.
7. Reference Points: displays the sizes of each of the following discrete tables. These limits are fixed and not configurable by the user. Figure 1 shows the current limits but these may change with future firmware releases.
   a. Input %I – the size of the input table in bits.
   b. Output %Q – the size of the output table in bits.
   c. Internal %M – the size of the internal memory in bits.
   d. Temporary %T – the size of temporary memory in bits.
   e. System %SA – the size of status bit memory bank A in bits.
   f. System %SB – the size of the status bit memory bank B in bits.
   g. System %SC – – the size of the status bit memory bank C in bits.
   h. System %S – – the size of the status bit memory in bits.
   i. Genius %G – the size of the Genius memory in bits.
   j. Total Discrete Memory – the total number of discrete bits available to the user.

After pressing the "Refresh PLC Status" button, the page is re-loaded from the PLC with the latest status values. If the data from the PLC is not available or there is an error in retrieving the data, the table cell associated with this data will be left blank.

2.3.2.1. Status Line

The browser status line for this page will show the PLC Mode, PLC Sweep Time, PLC Program Name and PLC Date/Time in the following format:

"PLC Mode: Stop I/O Enabled PLC Sweep Time: 2.5 msec Program Name: TEST1 PLC Date/Time: [redacted] [redacted]/13:51:16"

This represents the status of the PLC when the web page was loaded. In addition, the status line is updated when the "Refresh PLC Status" button is pressed.

2.3.2.2. Decimal Separator and Date Format

If the user presses the button labeled "Specify Decimal Separator and Date Format", the following dialog will appear:

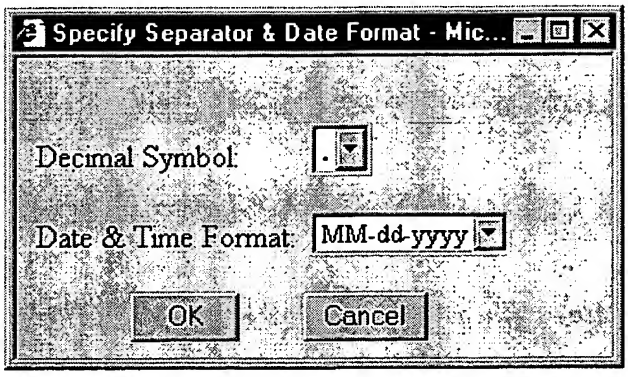

Figure 3 – Decimal Separator and Date Format Dialog

The user can select the decimal point separator and the date format from the two drop down boxes shown in the Figure below.

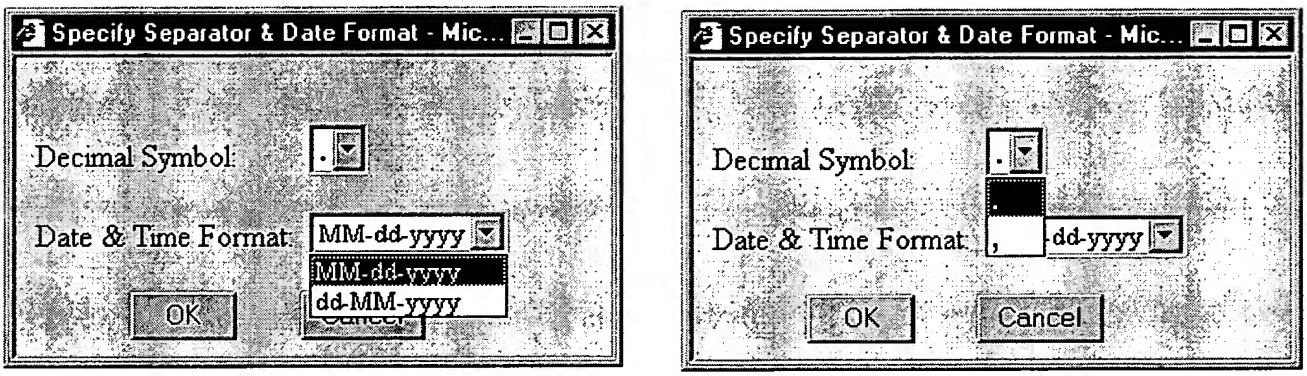

Figure 4 – Decimal Separator and Date Format Drop Down Boxes

In the first drop down box the user can select either a period or comma for the decimal point separator which will be used for any number requiring a decimal point on all web pages specified in this document. In the second drop down box the user can select either "MM-dd-yyyy" or "dd-MM-yyyy" date format which will be used for any date on all web pages specified in this document. After making the desired selection and pressing the "OK" button, the selections will be saved in a cookie so that they will be remembered the next time the same user on the same PC accesses these pages. The default will be a period for the decimal separator and "MM-dd-yyyy" for the date format. If the user presses the "Cancel" button, the selections will remain unchanged.

2.4. Reference Table Viewer

2.4.1. SRD Requirements

This web page meets the following SRD requirements described in section 4.30.2.

1. Reading and Display of PLC Reference Tables from a Browser over the Web shall be supported.

2.4.2. Description

By selecting the hyperlink, "View Reference Tables", the user can view a single reference table or customize a 6x10 table to view a mixture of references. In addition, the user can customize the number format for each cell. By default, the reference table viewer will show the values of the %R tables from %R1 to %R60 in a signed decimal format. However, if the user has previously accessed this web page on the same PC, the reference table viewer will first display the default settings and then immediately display the last table settings requested by the user in the previous session. These last table settings will be stored on the user's PC as a cookie.

An example page is shown below with a mixture of word and discrete references:

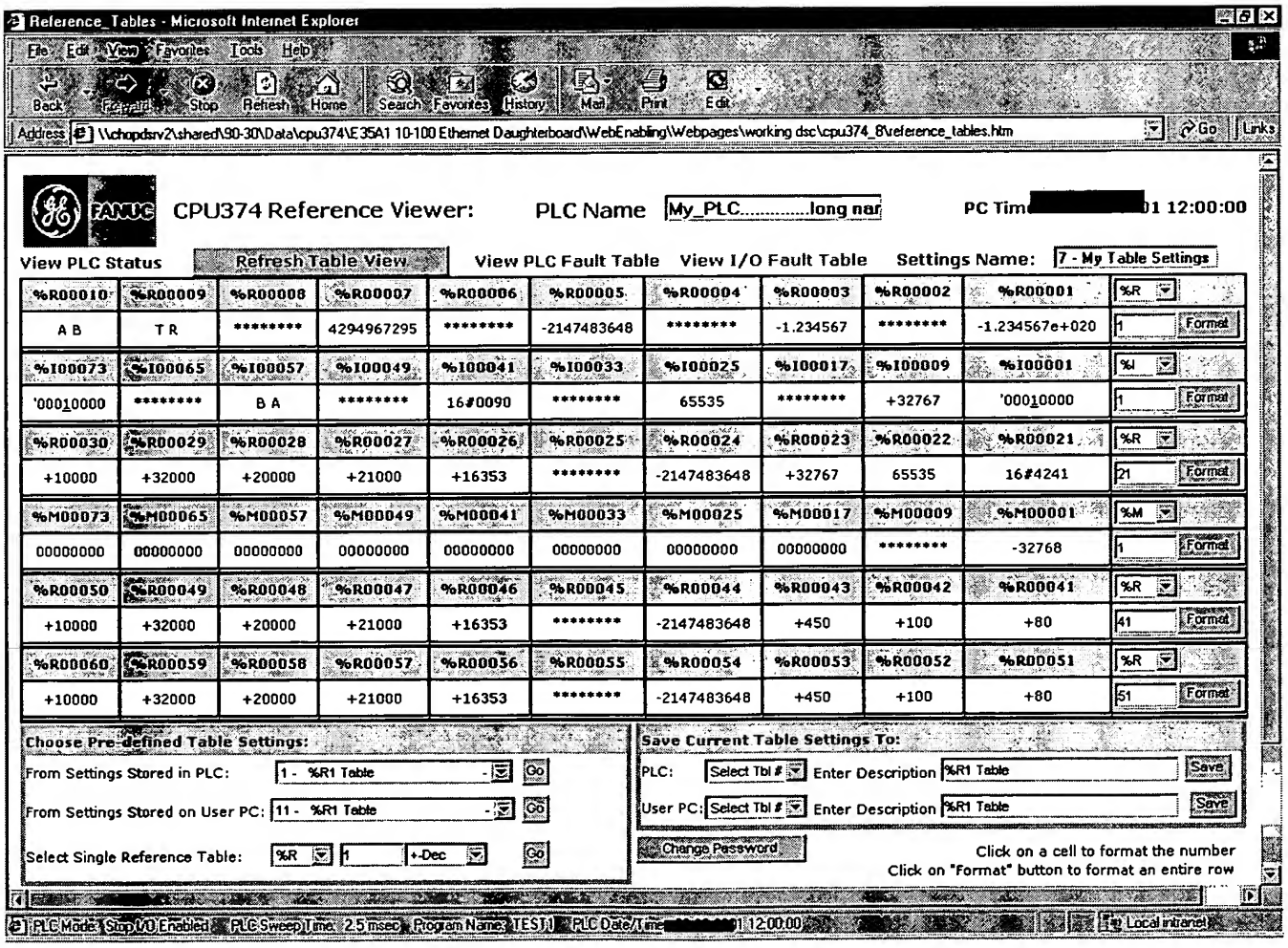

Figure 5 - Reference Viewer

The user can select one of the links at the top of the page to navigate to other pages supported by the CPU374 (View PLC Status, View PLC Fault Table or View I/O Fault Tables). In addition, the PLC name is shown in the textbox at the top of the page and the PC time when the page was loaded is shown in the upper right hand corner.

2.4.2.1. Basic Operation

The reference values in the 6x10 table are updated by selecting the "Refresh Table View" button. The values in the table will be determined by the reference table drop down box and the starting address in the textbox for each row. For example, if the first row drop down box shows %R and the address textbox shows 1, the first row will contain values for %R00001 through %R00010. The possible table values in the drop down box will be %R, %AI, %AQ, %I, %Q, %M, %T, %G, %S, %SA, %SB, %SC. The starting reference address textbox will allow integer entry from 1 to 99999. If a value is chosen outside of this range, the user will be asked to correct the number when they either leave the cell or when they choose to update the table. If the user specifies an address that is not available in the PLC, the value for that particular cell will be show blank "". If the user enters an address on a non-byte boundary for bit type tables (%I, %Q, etc), the starting address will be adjusted to the next lowest byte boundary address. For example if the user enters %I with starting address 3, the browser will adjust the start address to %I00001. However since future user defined web pages may not implement byte-alignment correction, the server should accept non-byte-aligned addresses and provide the value based on the next lowest byte-aligned address.

For word type memory (%R, %AI, %AQ) each row will contain 10 cells representing the next 10 consecutive word addresses in a right to left direction beginning with the starting address specified in the row's textbox (for example %R1 through %R10 for a starting address of 1). For bit type memory (%I, %Q, %M, etc) each row will contain 10 cells representing the next 10 consecutive byte aligned bit addresses in a right to left direction (for example, %I00001, %I00009, %I00017 ..... %I00073 for a starting address of %I00001).

The user will see the following dialog when they click on a reference table address cell above the reference value (for example clicking on the "%R00010" link in the figure above causes the following dialog to appear).

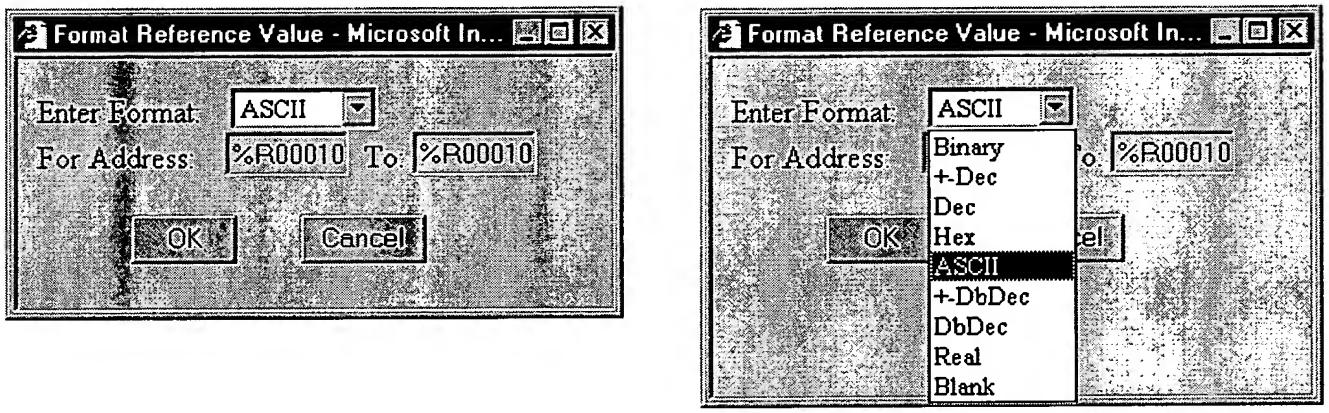

Figure 6 - Formatting Dialog Box

This dialogue provides a drop down box to select the number format for the selected reference address. In addition, it shows the reference address or addresses being formatted. The possible format selections are: Binary, +-Dec, Dec, Hex, ASCII, +-DblDec, DblDec, Real, and Blank. The default format for word type memory (%R, %AI, %AQ) will be +-Dec and the default for bit type memory (%I, %Q, %M etc.) will be Binary. The drop down box will show the current format as the selected item. For example if the cell value for %R10 is selected and that cell's current format is "Hex", the drop down box will show "Hex" as the selected item. After pressing the "OK" button, the format of the current value will be immediately changed by the browser to the new format if Internet Explorer is used. For the Netscape browser, the format will change after the user refreshes the screen. If the user presses the "Cancel" button, the previous format will continue to be displayed. The user can also supply the format for an entire row by pressing the "Format" button for a particular row. This will bring up the same formatting dialog but it will show a range of reference addresses as shown below:

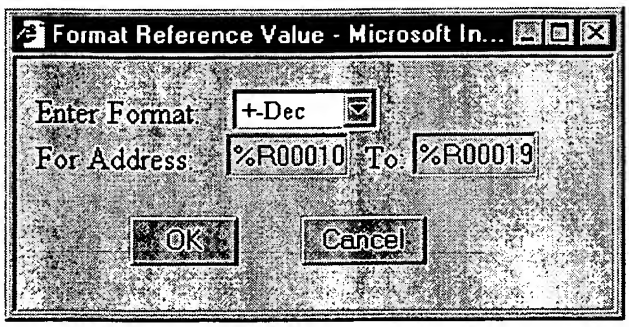

Figure 7 – Format Dialog For An Entire Row

In general when auxiliary dialogs are presented to the user, the dialogs will be placed in the middle of the user's overall PC screen for ease of entry.

The meaning and the limitation for the various formats are discussed below.

1. Binary: uses a 1 or 0 to show the binary representation of one byte (8 bits) of data at the specified address for bit type memory (%I, %Q, %M etc) or one word (16 bits) for word type memory (%R, %AI, %AQ). If a discrete bit is overridden for the %I, %Q, %M or %G tables, the bit will underlined in the display.
2. +-Dec: signed decimal for one word of data (16 bits) at the specified address. Valid ranges are from –32768 to +32767.
3. Dec: this is unsigned decimal for one word of data (16 bits) at the specified address. Valid rages are from 0 to 65535.
4. Hex: provides a four digit hexadecimal value for one word of data (16 bits) at the specified address. Valid ranges are from 16#0000 to 16#FFFF. The value will have 16# as a prefix (for example 16#4241).
5. ASCII: ASCII representation of two 8-bit values (16 bits) at the specified address. For example, a hex value of 16#4142 will be presented as "A B". For each 8 bit value, the character shown for hex values from 00 to 7F will be the same as Logicmaster (see Logicmaster 90-30/20/Micro Programming Software User's Manual – September 1998 GFK-0466L p.4-14). For hex values between 80 and FF, the character displayed will be as shown in Appendix 1. Since Netscape 4.0 does not support character code to ASCII conversions, ASCII format will not be supported for this version and the user will be informed they need Internet Explorer 4.0 or Netscape 4.7 or later to use the ASCII format. If a Netscape 4.0 user selects a set of saved settings that contain ASCII formats, the default format will be displayed.
6. +-DblDecimal: signed decimal for a double word (32 bits) at the specified address. Valid ranges are from -2,147,483,648 to +2,147,483,647. This format is only available for word type memory (%R, %AI, and % AQ).
7. DblDecimal: unsigned decimal for a double word (32 bits) at the specified address. Valid ranges are from 0 to 4,294,967,295. This format is only available for word type memory (%R, %AI, %AQ).
8. Real: 7 decimal digits plus a decimal point and exponent if necessary (for example 123.4567, 1.234567e+038). This format uses 2 words or 32 bits. This format is only available for word type memory (%R, %AI, %AQ). The range of numbers is +-1.401298e-045 to +-3.402823e+038.
9. Blank: if the user selects blank, the associated cell will have no value or reference address header. If the user chooses "Blank" for an entire row, the reference address and value row will be blank with the exception of a "Format" hyperlink. If the user clicks on the "Format" hyperlink, the standard format dialog will appear which allows the user to change the format back to a non-Blank value (see Figure below: notice that row 3 is blank). When choosing the blank format for the entire row, the cell reference address and values will be immediately blanked as shown in the figure below:

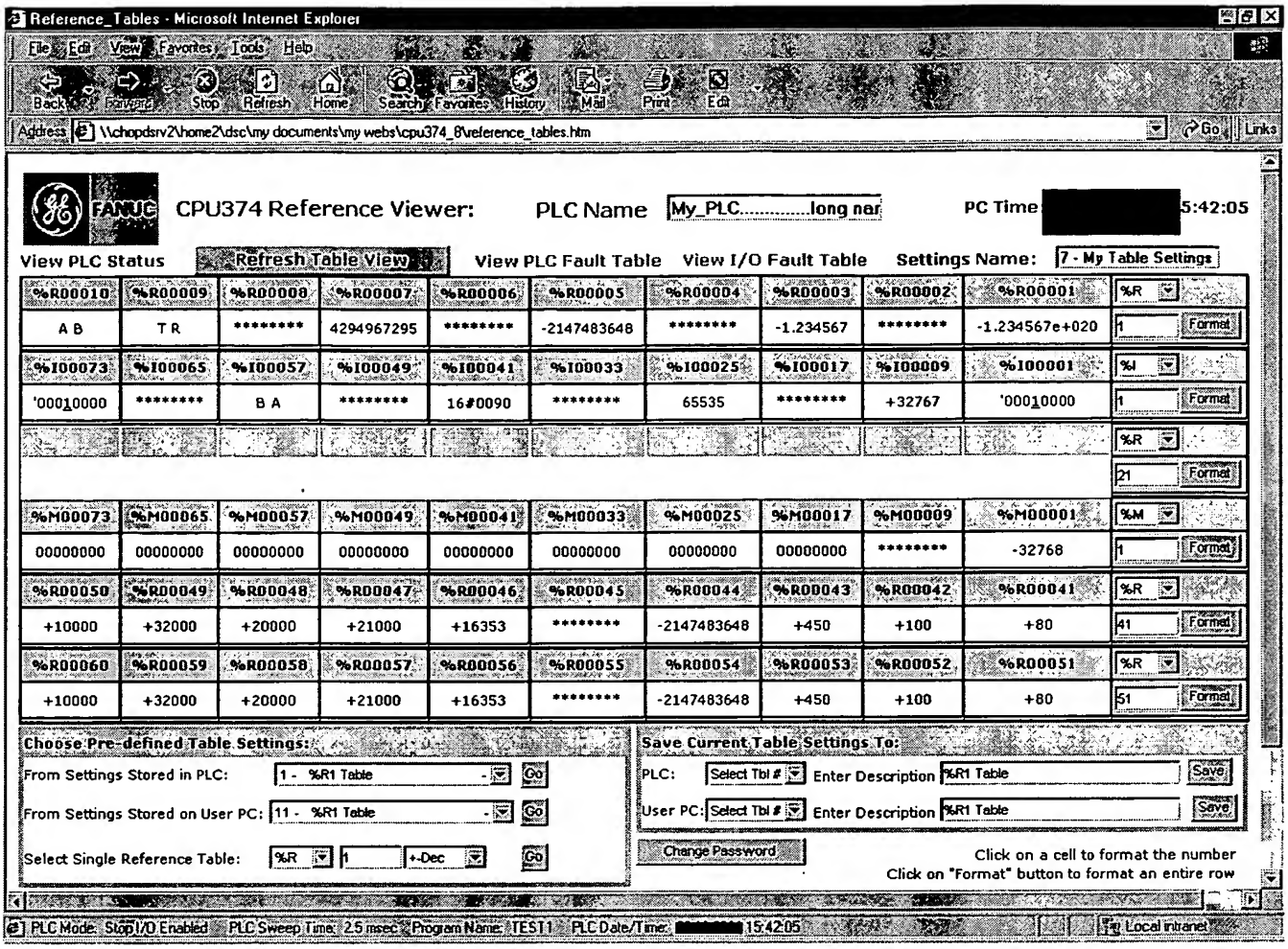

Figure 8 – Example of Reference Table With a Blank Row Before the Screen is Refreshed

After the screen is refreshed, a blank row's height will be decreased as shown in the example below for row 3.

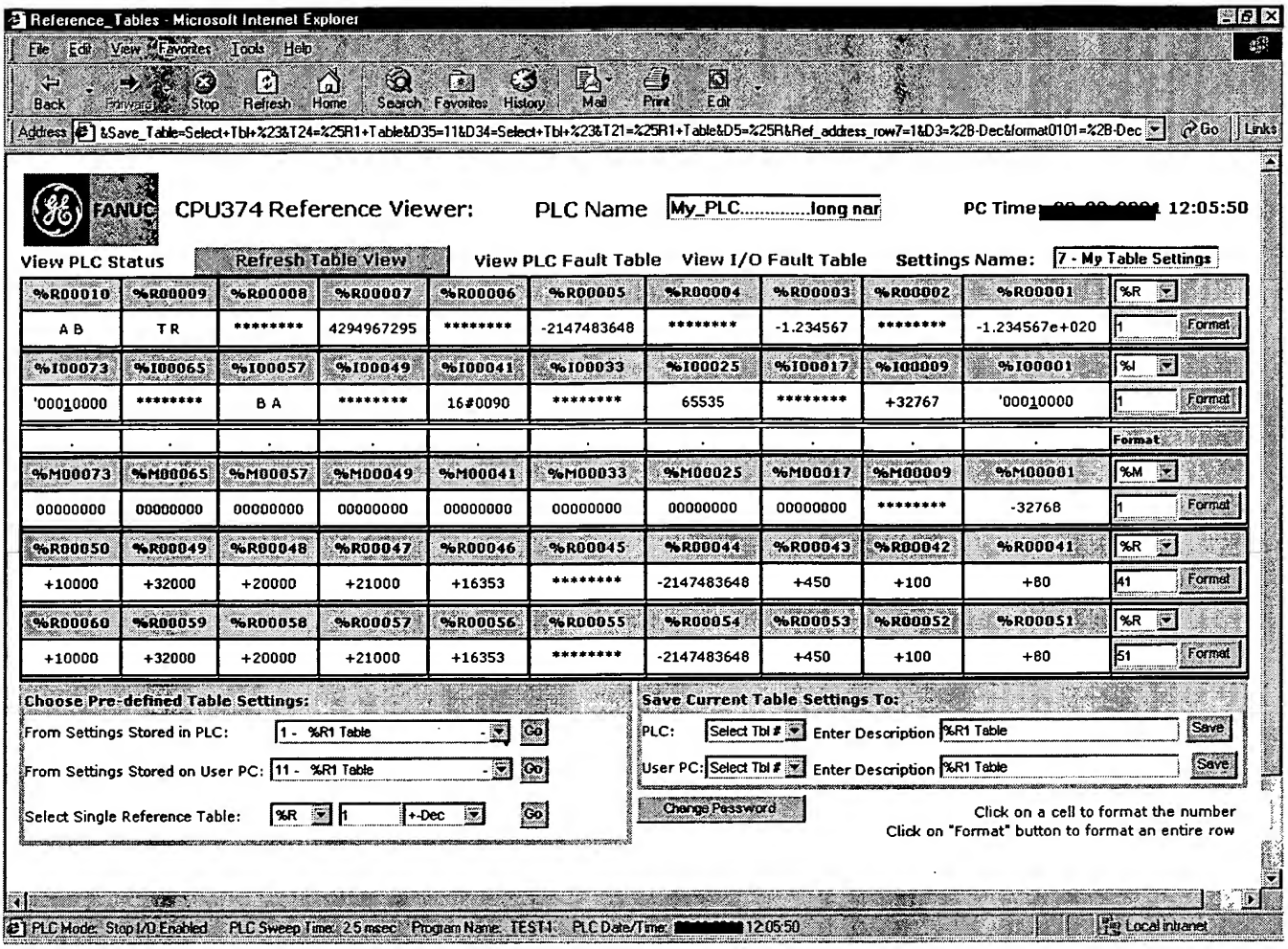

Figure 9 – Reference Table with 3rd Row Blank

Note 1: When a 16 bit format is chosen for bit type memory (for example +-Dec, Dec, Hex, ASCII), the value is displayed in the cell containing the least significant address and the adjacent cell containing the most significant address is filled with stars (******). For example if a cell for address %I00009 is formatted as signed decimal, the value will be displayed in the %I00009 cell (ex. +32767) and the cell for %I00017 will contain stars (see Figure 2 the second row). When a 32 bit format is chosen (word type memory only), the value is displayed in the cell containing the least significant address and the cell containing the most significant address is filled with stars (******). An example is shown in Figure 2 in the first row where %R1 is formatted as Real format.

Note 2: Comma separation for numbers greater than 999 will not be supported. For example, 1000 will not be shown as 1,000.

Note 3: If the user selects a format for a cell in the first column on the left (for example %R00010 in the figure shown above) and the format requires values from two different cells (for example, Real), the new format will be accepted since the web page will keep the 11th value internally. For example in row 1 of the "Reference Viewer" figure above, the %R00011 value will be kept internally so that it can be used to properly display the value of %R00010 when a two cell format is specified.

2.4.2.2. Save Current Table Settings

The user has the option of saving the current table settings (reference table, starting address for each row and the number formats for each cell). As described in further detail below, the user can either save these settings to the PLC or to the user's PC.

1. Save Current Table Settings To: PLC: if the user presses the "Save" button to the right of the label "PLC", the reference table, starting addresses for each row and the formats for each value cell are saved in the CPU374 module and the reference table values are updated in the table. Up to 10 different settings can be saved to the module (labeled 1 through 10). The possible settings numbers are specified in the drop down labeled as "Select Tbl #" in the figure below.

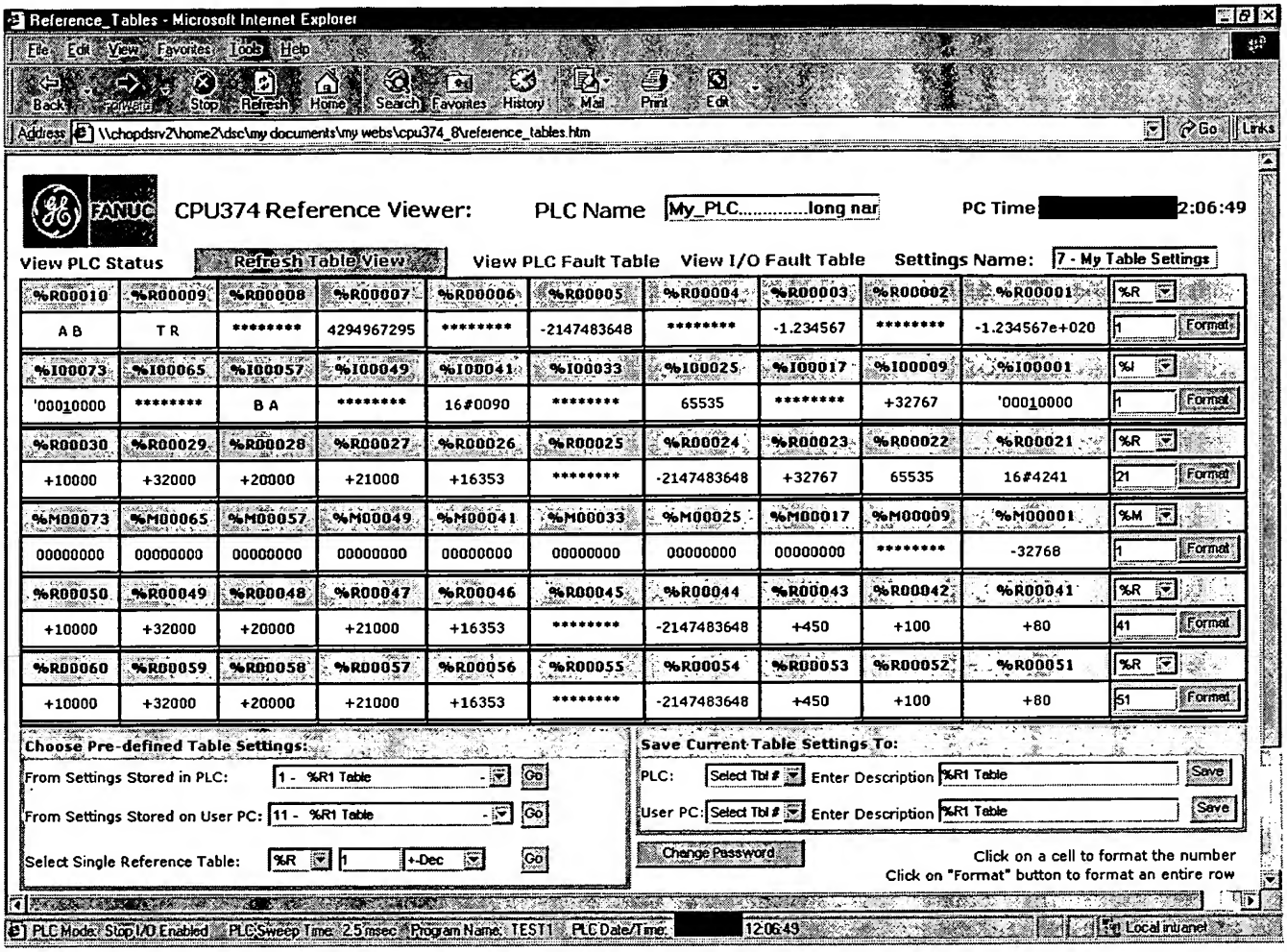

Figure 10 – Save Current Table Settings Screen

The user can also associate a description with a table setting in the "Description" textbox to the right of the drop down box. This description can contain any standard character (alphanumeric characters and the following other characters: ! @ # $ % ^ & * ( ) _ - + = { } | [ ] \ ~ ` : " ; ' < > ? , . /) with a length of 1 to 32 characters. The default value for the description will be "%R00001 Table" since this is the default reference table.

After pressing the "Save" button, the user will be presented a Reference Viewer password dialog as shown in the figure below if passwords have been set to a non-blank value.

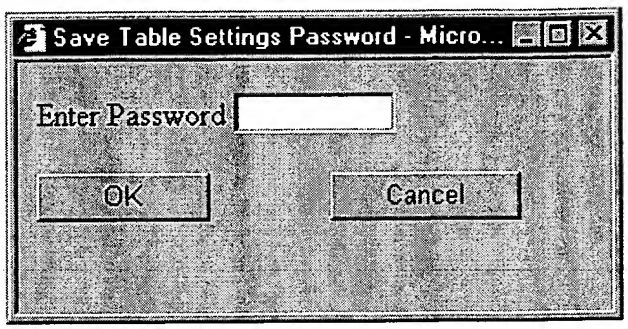

Figure 11 - Password Dialog

The user needs to enter the correct password and press the "OK" button to proceed. As the user enters the password, the star character "*" will be displayed for each character so that the password cannot be seen by another user. If the user presses the "Cancel" button, the settings will not be saved and the values in the table will not be updated. The default password for the module will be blank (""). The password field will accept up to 10 characters and will use the same character set as the description field. The password will be case insensitive.

If the current Reference Viewer password is blank (""), the user will not be required to enter a password to store a new setting and the password dialog will not be presented.

If the user enters the wrong password, the new settings will not be stored in the module and as a result the description associated with that setting will not show up in the drop down box next to the "From Settings Stored in PLC" label. In addition, the text in the textbox next to the label "Settings Name" will not be updated. However, the values in the table will be updated.

If the user enters the correct password, the current table settings will be saved in the PLC, the description associated with the setting number in "From Settings Stored in the PLC" drop down box will be shown and the values in the table will be updated. In addition, the textbox at the top of the page will show the new table setting number and the description. For example, the user wants to save the current reference tables, starting addresses and formats in settings #7 with the description "My Table Settings". The user selects "7" from the drop down box, enters the description "My Settings" in the textbox. Before pressing the "Save" button, the drop down box next to the label "From Settings Stored in PLC" would show #7 as "7 - %R1 Table" (this is the default). After pressing the "Save" button, the drop down box will show #7 as "7 – My Table Settings" and the textbox at the top of the page will show "7 – My Table Settings" indicating the table settings have been saved in the module.

The user also has the option to change the Reference Viewer password by pressing the "Change Password" button. The user is presented the following dialog in this case:

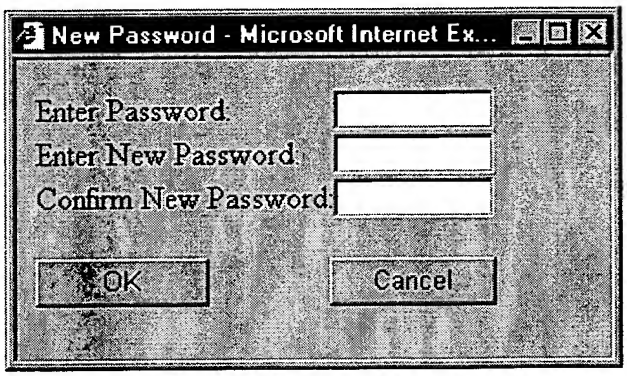

Figure 12 - Change Password Dialog

In order to change the password, the user must enter the current password, the new password, a confirmation of the new password and then press the OK button. If the new password is confirmed and the user enters the correct current password, the new password will be saved in the module and the values in the table will be updated. If the user either presses Cancel or does not confirm the new password, the change password operation is canceled, the change password dialog closes and the user must re-start the change password sequence.

If the user loses the Reference Viewer password, the password can be reset by downloading an AUP file that contains a new password. The format for the line in the AUP file line will be:

ref_password = my_paswrd

In addition, the user can change the Reference Viewer password (for example to "my_paswrd") through the station manager by entering the following command:

CHPARM ref_password my_paswrd

Note 1: Since the reference viewer password is case insensitive, double quotes are not required to preserve the capitalization of the CHPARM ref_password argument.

Note 2: the CHPARM commands are not available if the PLC has received a valid configuration from the programmer.

2. Save Current Table Settings To: User PC: – the user can similarly save and recall their settings on their local PC hard drive as a cookie associated with the logged on user. The user can select from 10 settings numbered 11 to 20 with a description for each setting. To save the settings, the user selects a table settings number from the drop down box to the right of the "User PC" label, enters a description in the textbox and presses the "Save" button. This operation also updates the values in the table. Password verification is not needed in this case. These settings are immediately saved on the user's PC and immediately available to the user as one of the pre-defined table settings. In addition if the user subsequently opens this web page logged on as the same user on the same PC, these saved settings will be immediately available.

2.4.2.3. Choose Pre-Defined Table Settings

The user has the option of using pre-defined table settings that set the reference table, starting address for each row and the number formats for each cell. There are three types of pre-defined tables discussed below.

1. Choose Pre-defined Table Settings From Settings Stored in PLC - the user can select from a list of saved table settings from the drop down box to the right of the label "From Settings Stored in PLC". The items in the drop down box are labeled with a setting number and a user description. If the user presses the associated "Go" button, the table is updated with the saved settings (reference table, starting addresses for each row and format for each cell) and the values in the table are updated from the PLC. If the user selects a setting that has never been saved to the module, then the settings will default to the %R table with starting address 1, 11, 21, 31, 41, 51 for each row respectively and signed decimal format. The textbox at the top of the page will show the current table setting and description that is being displayed.

2. Choose Pre-defined Table Settings: From Settings Stored on User PC: If the user has previously saved table settings to their PC, these settings can be retrieved by first selecting one of the saved settings from the drop down box and pressing the "Go" button. This will retrieve the reference table, the starting address values for each row and the format for each cell and then update the values in the table using these settings. The textbox at the top of the page will show the current table setting and description being displayed.

3. Choose Pre-defined Table Settings: Select Single Reference Table –to quickly view a section of one particular reference table in the PLC, the user can select the reference table, the starting address and format in the drop down boxes and textboxes to the right of the "Select Single Reference Table" label. After pressing the "Go" button, the table will be updated with the values for the 60 consecutive reference addresses following the start address for word type memory and the next 480 reference addresses for bit type memory. In addition, the textbox at the top of the page will show the beginning table reference address followed by the word "Table" (for example, "%R00001 Table"). For example if the user selects the %R table, starting address 1, signed Decimal format and presses the "Go" button, row 1 will show %R with starting reference 1, row 2 will show %R with starting reference 11 and so forth. The textbox at the top of the page will show "%R00001 Table" and the format for all cells will be signed Decimal.

2.4.2.4. Settings Name Textbox At Top of Page

When the reference view page first opens, the table settings textbox at the top right hand corner of the page will display the default table description "%R00001 Table". If the page has been previously accessed by the same user on the same PC, the browser will then retrieve the last table settings from the previous session from the user's PC via a cookie and refresh the page with these settings including the previous value in the "Settings Name" textbox . . If the user selects a pre-defined saved table, the pre-defined table number and description will be shown. For example if the user selects "7 – My Table Settings" from the drop down list of pre-defined tables and presses the associated "Go" button, the text "7 – My Table Settings" will be displayed in the textbox. This textbox will show "Not Saved" if the user changes any of the settings in the table and presses the "Refresh Table View" button since the current settings will not represent one of the saved settings. If the user selects a single reference table, the textbox will contain the starting reference address followed by the word "Table" (for example %R00001 Table).

2.4.2.5. Status Line

The browser status line for this page will show the same information as specified in the PLC Status section.

2.4.2.6. Special Conditions

The purpose of this section is to specify the behavior under special conditions.

1. More than one user trying to save settings to the PLC: If two users access the web server from two different PCs, a conflict is possible when saving table settings to the PLC. For example, User #1 decides to save table settings to settings #3 with a description of "User #1's Settings". Simultaneously, User #2 on another PC decides to save his or her settings to settings #3 with a description of "User #2's Settings" to the same PLC. In this case, it cannot be guaranteed which of the settings will be saved to the module. The server will simply take the last received request and overwrite the previous settings for that particular settings number.

2.5. Fault Tables

2.5.1. SRD Requirements

This web page meets the following SRD requirements described in section 4.30.2.

2. Reading and Display of PLC and IO Fault Tables from a Browser over the Web shall be supported.

2.5.2. Description

There will be two fault table pages: PLC Fault Table and I/O Fault Table. When the user selects the "View PLC Fault Tables" link, the user will see the PLC Fault Table shown here.

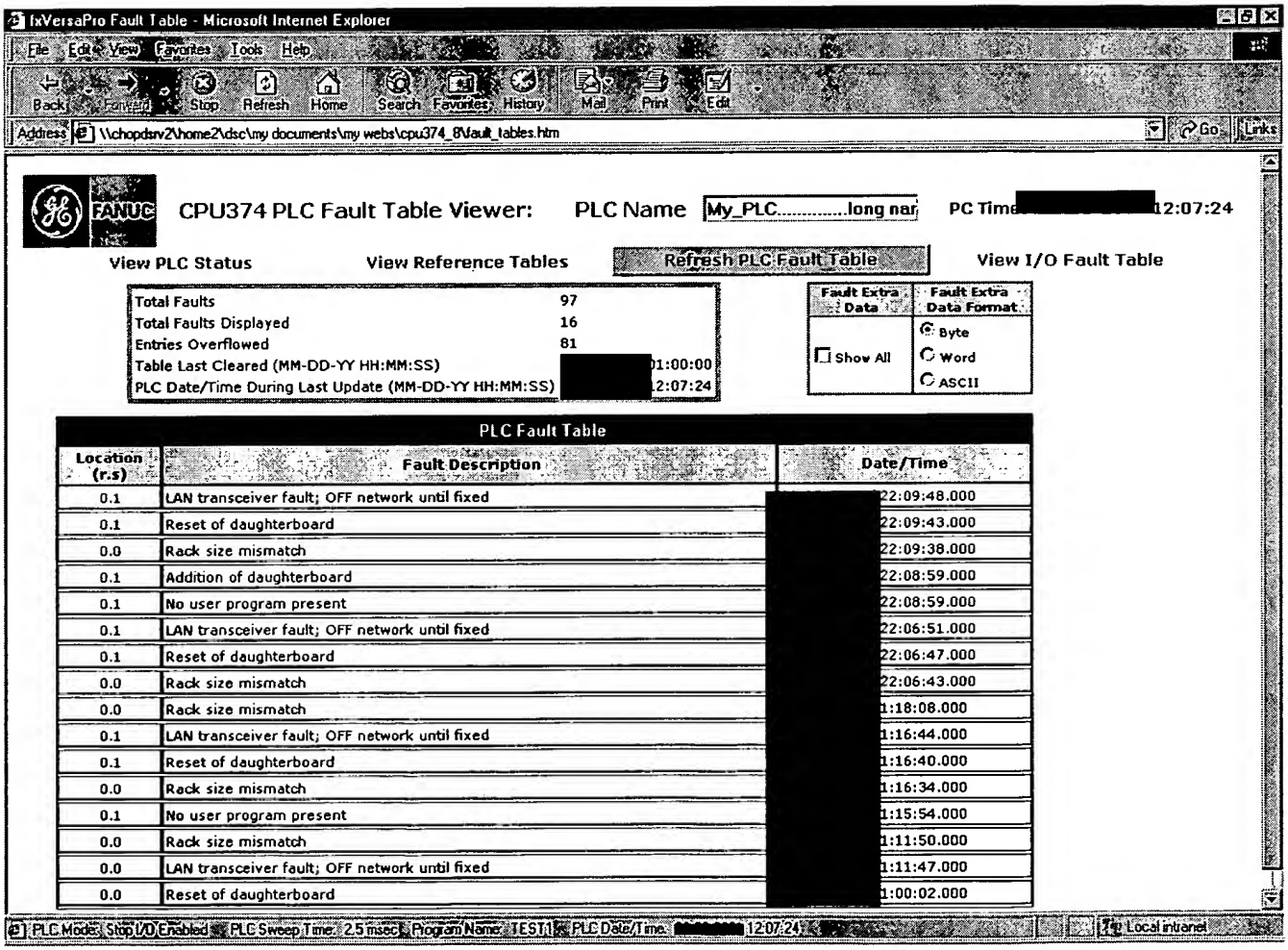

Figure 13 - PLC Fault Table Without Fault Extra Data

The user can select links to the other CPU374 pages by selecting the appropriate link as shown in the preceding Figure. Pressing the "Refresh PLC Fault Table" button will update the screen with the latest PLC fault information. In addition, the PLC name will be shown at the top of the page and the time stamp of the PC will be recorded in the upper right hand corner in the same manner as the View PLC Status page. The PLC fault table provides up to 16 entries arranged from newest to oldest. If there are fewer than 16 entries, the remaining rows will be blank. If there are more than 16 faults, the table displays the most recent faults in the first 8 rows and the oldest faults in the last 8 rows. This table provides the same information

displayed by the VersaPro and the Control Fault Table application when the PLC fault table is first opened. When using Internet Explorer, the fault extra data can be viewed by using the mouse to highlight a particular fault and then clicking on the fault. This is shown in the figure below:

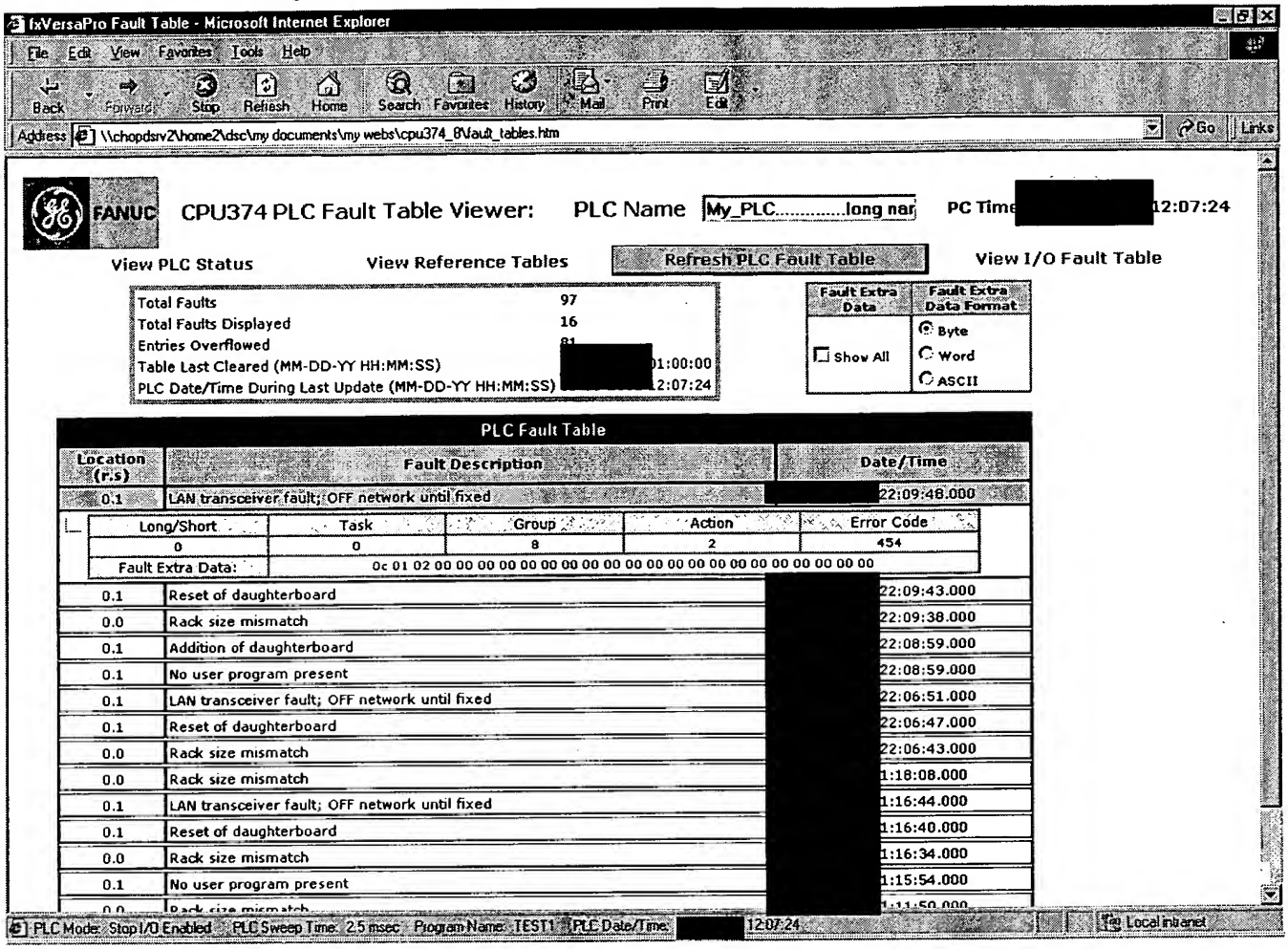

Figure 14 – Clicking on Fault to Get Fault Extra Data

The fault extra data can be displayed in byte, word or ASCII format depending on which radio button is selected at the top of the screen. These selections affect the display of all fault extra data. If an error code does not have a string associated with it, the "Fault "Description" field will be blank. The user can also show the fault extra data for all faults by selecting the "Show All" checkbox as shown in the figure below:

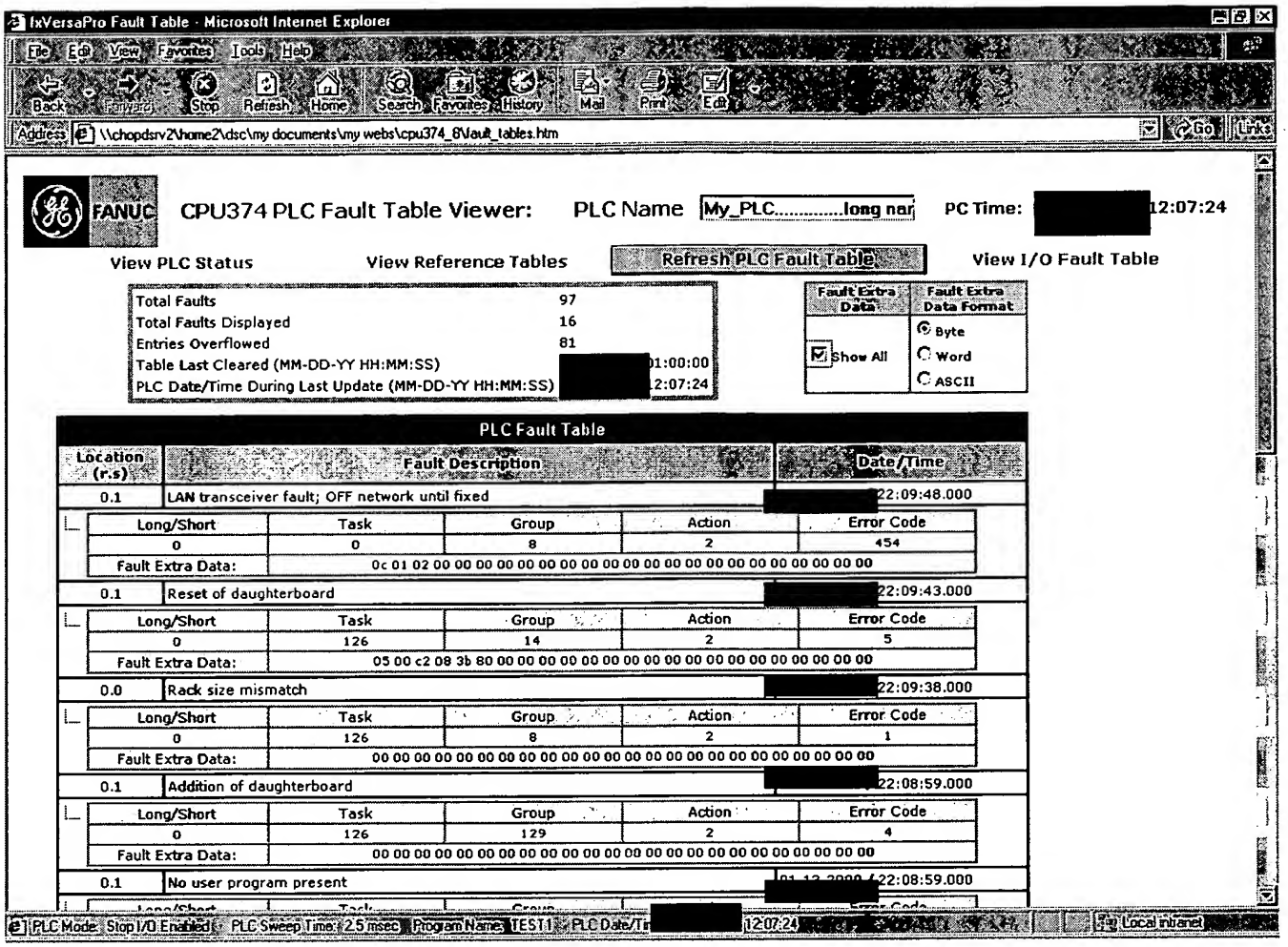

Figure 15 – Showing All Fault Extra Data

In order to see fault extra data, Netscape users must first check the "Show All" checkbox and press the "Refresh PLC Fault Table" button. This will show the fault extra data for all faults. Netscape users do not have the option of showing fault extra data for selective faults. To hide the fault extra data, Netscape user's must uncheck the "Show All" checkbox and again press the "Refresh PLC Fault Table" button.

The I/O Fault Table is shown below:

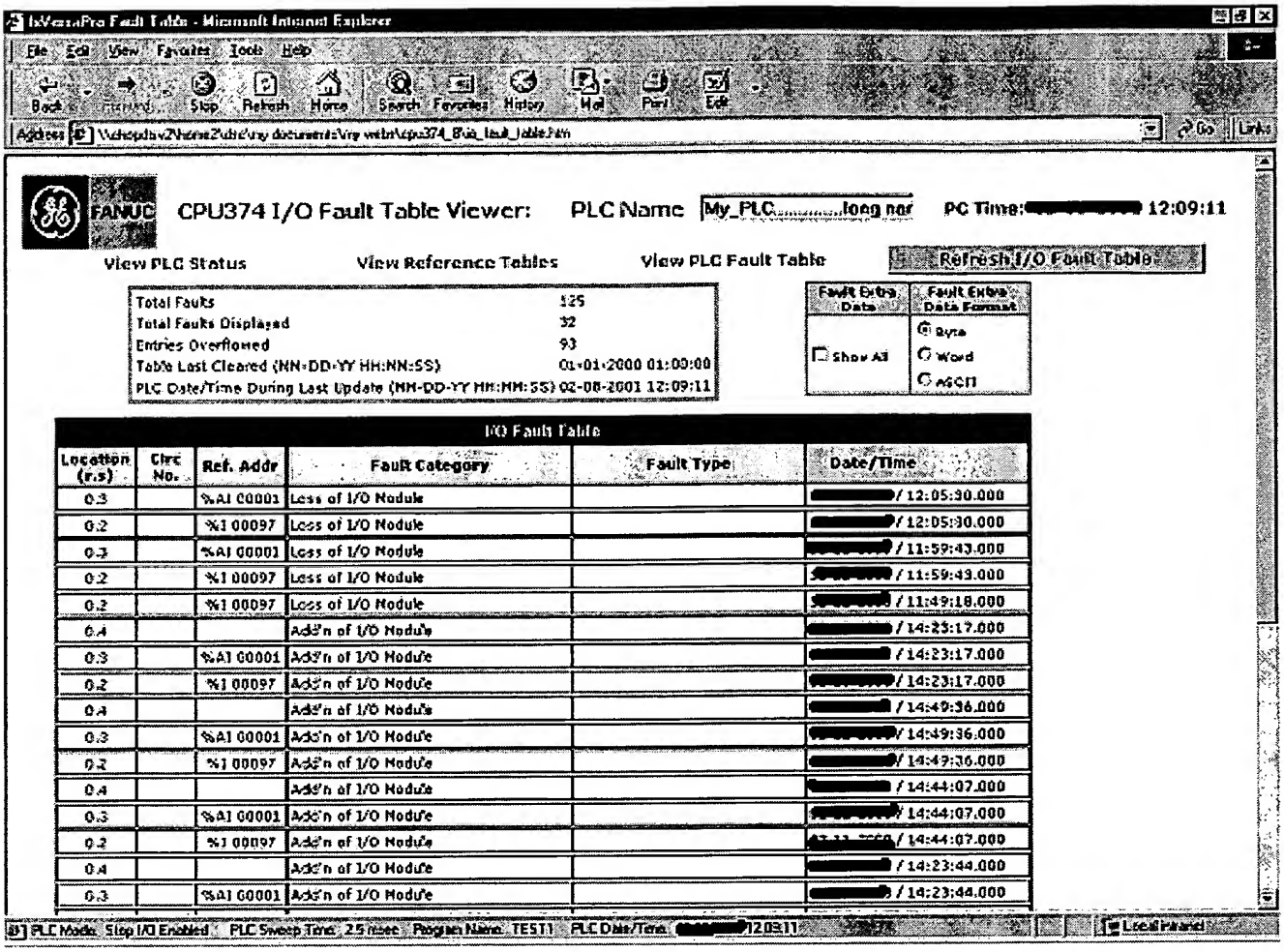

Figure 16 - I/O Fault Table

Similarly, this page provides links to other CPU374 web pages. The "Refresh I/O Fault Table" button will update the screen with the latest information from the PLC. This screen provides a table that can display up to 32 I/O fault entries arranged from newest to oldest. If there are fewer than 32 entries, the remaining rows will be blank. If there are more than 32 faults, the table displays the most recent faults in the first 16 rows and the oldest faults in the last 16 rows. Similarly, this table provides the same information displayed by the VersaPro and Control Fault Table application when the I/O Fault Table is first opened. The fault extra data is displayed in the same manner as the PLC fault table. An example with all fault extra data displayed is shown below:

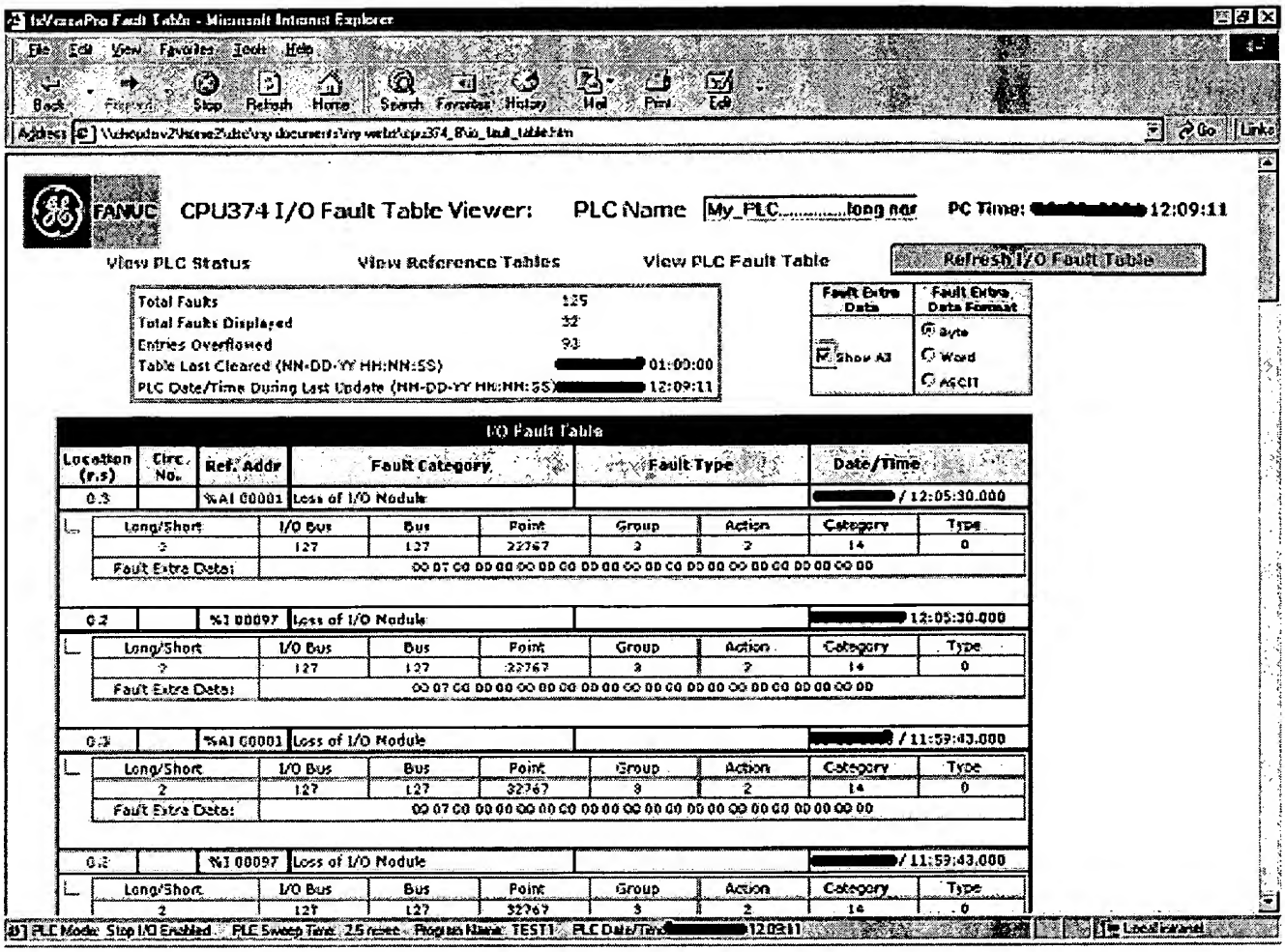

Figure 17 – I/O Fault Table with Fault Extra Data Displayed

If a Fault Category or Fault Type Description do not have a string associated with them, the fields will be blank.

The PLC name and PC time stamp are shown at the top of the page in the same manner as the other pages.

The status line of the PLC and I/O Fault pages will show the same information as the PLC Status page and is updated when the "Refresh I/O Fault Table" or "Refresh PLC Fault Table" is pressed.

2.6. Internationalization & Branding

2.6.1. SRD Requirements

This web page meets the following SRD requirements described in section 4.30.2.

4. Internationalization of the character strings displayed by the Browser during fault or reference table display shall be supported

2.6.2. Description

The initial web pages and fault string files (fault code and fault type strings) developed for this project will be United States English and GE Fanuc branded.

The fault string file will be derived from the VersaPro and Control Fault Table application resource files which are available in English, Spanish, German and French. Once the U.S. English web pages are finalized for release, translations will be generated for each file in the following languages: Spanish, French and German. Strings requiring translation will be located in one section of the U.S. English web pages to make it easy for the translator to substitute language specific strings.

GE Fanuc branded elements will be set-up so that changes to one section of a page can be made to modify it to another brand. A set of brand neutral pages will be generated to support customers who use branded product such as ALSTOM.

As described at the beginning of this document, customers will then ftp to the PLC the set of web pages and fault strings that meet their language and/or branding needs.

To further support internationalization, the user also has the option to specify the decimal point separator as either a period or a comma and to specify the date format as MM-DD-YYYY format or DD-MM-YYYY as described on the View Status Page,

2.7. Performance Requirements

All pages should load 30 seconds or faster when the user is using a 28.8Kbaud modem and proportionally faster depending on the user's effective connection baud rate but not guaranteed to be faster than 6 seconds. The 6-second specification will be tested under the following PC and browser conditions

1. PC connected to the PLC via Ethernet at 10MB network speed.
2. No other web browser applications or other applications actively using the same Ethernet connection
3. PC with Pentium 166Mhz or better, Windows NT 4.0 SP5 Operating System, 64Mbytes RAM and 50Mbytes free disk space.

and under the following PLC conditions:

1. CPU sweep time 100ms or less.
2. 8 SRTP server/channel connections:
   a. 4 write requests with a period of 1 second and a length of 512 words.
   b. 4 read requests with a period of 1 second and a length of 512 words.
3. 32 EGD exchanges:
   a. 4 produced exchanges with a period of 200ms and length of 200 bytes.
   b. 4 consumed exchanges with a period of 200 ms and length of 1000 bytes.
   c. 12 produced exchanges with a period of 1 second and length of 500 bytes.
   d. 12 consumed exchanges with a period of 1 second and length of 1400 bytes.
4. 1 programmer attached to the PLC via Ethernet and monitoring reference tables on a different PC than the browser PC.
5. 1 switch and 2 routers between the browser's PC and the PLC. The router systems should only be involved in routing data between the browser's PC and the PLC and should otherwise be idle.
6. Network load of less than or equal to 15% tested at 10MB network speed.
7. Only one browser attempting to access pages from the server

2.8. Web Page Memory Size

The CPU374 module will have 1.5Mbytes available for both GE Fanuc developed pages and user developed pages in the future.

Appendix 1 – Characters Displayed in ASCII Format

The character shown in ASCII format for hex values from 00 to 7F will be the same as Logicmaster (see Logicmaster 90-30/20/Micro Programming Software User's Manual – [redacted] GFK-0466L p.4-14). Note the 7F code shows the delta symbol (?) for Logicmaster.

For hex values from 80 to FF, the following characters will be shown. In instances where Netscape is different, the differences are shown in parenthesis.

Bit Pattern (Hex)	Character (Netscape)	Bit Pattern (Hex)	Character (Netscape)	Bit Pattern (Hex)	Character (Netscape)	Bit Pattern (Hex)	Character (Netscape)
80	blank( )	90	blank	a0	blank	b0	blank( )
81	^Á	91	^Ñ	a1	¡	b1	±
82	^Â	92	^Ò	a2	¢	b2	²
83	^Ã	93	^Ó	a3	£	b3	³
84	^Ä	94	^Ô	a4	¤	b4	´
85	^Å	95	^Õ	a5	¥	b5	µ
86	^Æ	96	^Ö	a6	¦	b6	¶
87	^Ç	97	^×	a7	§	b7	·
88	^È	98	^Ø	a8	¨	b8	¸
89	^É	99	^Ù	a9	©	b9	¹
8a	^Ê	9a	^Ú	aa	ª	ba	º
8b	^Ë	9b	^Û	ab	«	bb	»
8c	^Ì	9c	^Ü	ac	¬	bc	¼
8d	^Í	9d	^Ý	ad	blank	bd	½
8e	^Î	9e	^Þ	ae	®	be	¾
8f	^Ï	9f	^ß	af	¯	bf	¿

Bit Pattern (Hex)	Character (Netscape)	Bit Pattern (Hex)	Character (Netscape)	Bit Pattern (Hex)	Character (Netscape)	Bit Pattern (Hex)	Character (Netscape)
c0	blank ( )	d0	blank	e0		f0	
c1	Á	d1	Ñ	e1	á	f1	ñ
c2	Â	d2	Ò	e2	â	f2	ò
c3	Ã	d3	Ó	e3	ã	f3	ó
c4	Ä	d4	Ô	e4	ä	f4	ô
c5	Å	d5	Õ	e5	å	f5	õ
c6	Æ	d6	Ö	e6	æ	f6	ö
c7	Ç	d7	×	e7	ç	f7	÷
c8	È	d8	Ø	e8	è	f8	ø
c9	É	d9	Ù	e9	é	f9	ù
ca	Ê	da	Ú	ea	ê	fa	ú
cb	Ë	db	Û	eb	ë	fb	û
cc	Ì	dc	Ü	ec	ì	fc	ü
cd	Í	dd	Ý	ed	í	fd	ý
ce	Î	de	Þ	ee	î	fe	þ
cf	Ï	df	ß	ef	ï	ff	ÿ

Figure 18 – Characters Displayed for corresponding 80 through FF hex values when using ASCII format

[End of document]

APPENDIX C

Board Hardware Description

90-30 10/100base-T Embedded Ethernet Controller

E35A1
&
E35B1

Rajesh Hiranandani

PRODUCT DEVELOPMENT

GE FANUC AUTOMATION NORTH AMERICA, INC
Charlottesville, Virginia

CLASS 3 DOCUMENTATION

PROPRIETARY INFORMATION

Approval	Date	
Author: Rajesh Hiranandani	[redacted]	**GE FANUC Automation North America, Inc.** Charlottesville, Virginia
Issued/Re-issued:		**E35A1 Board Description**
Distribution: ***INTERNAL USE ONLY***	Dwg No 44A747987	Sheet **1 of 24**

Version	Date	Page-paragraph	Remarks
0.1	[redacted]		Initial Version
0.2	[redacted]	Changed	Dual Port replaces the ENI Interface
0.3	[redacted]	Changed	Added additional Chip Select for SDRAM for Data & Code, Updated the Motherboard connector
0.4	[redacted]	Changed	Changes from the Board Design Review. Refer Review database for details.
0.5	[redacted]	Changed	Changed processor to SH2-7616, and replace Flash with SyncFlash
0.6	[redacted]	Changed	Changes from the Board Design Review. Refer Review database for details.

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1 OVERVIEW

This document describes the requirements for a new board, which is the 90-30 10/100base-T Embedded Ethernet Controller CPU product. It is a daughterboard and will be a part of the CPU 374 module alongwith the CY3A1 motherboard.

- Product line - 90-30.
- The E35A1 fab will be multilayer (10) and will use fine-line (8 mil) conductors on outer layers and ultra-fine-line (6 mil) on the inner layers. This fab contains the SH2-7616 processor and memory. The E35A1 form factor will facilitate 2 units per 8.7" x 11" fab panel.

2 APPLICABLE DOCUMENTS

Document	Drawing Number
Related Documents from the CPU364/CPU374 project:	
MFR - Series 90-30 374 CPU (10/100 MPBS Full Duplex Ethernet Interface), Rev 1.2, [redacted], Dave Hietanen	MFR_DJH cpu365_1_11
CPU 374 System Requirements Document, [redacted], Brad Bolfing	SRD_20000412_BJB_1
90-30 CPU374 H/W Product Requirements , [redacted], Owen Wells & Rajesh Hiranandani	PRD-001103-HIR
CPU360 Daughterboard Interface Specification, Rev 1.0, [redacted]	44A738995
CPU36x Motherboard (CX3A1) Board Description	44A739582
CX3A1 Board Elementary Diagram	44C744210
PLC Factory Test Services, D. Belcher, GE Fanuc internal document, [redacted].	44A963102
VersaMax Manufacturing Test Specification and Design for Testability Handbook, D. Belcher, [redacted].	44A962199
System Design for Automated MAC Address Programming and Verification, Bill Tunis & Dan Belcher, [redacted].	44A963160
MAC Address Serial EEPROM Specification, Scott Gaskins, [redacted].	44P725987-401D
SH2-7616 Hardware Reference Guide Manual, Hitachi, , Rev.0.5, [redacted]	-
Related Documents from the CPUE05 project:	
VersaMax CPU005/CPUE05 Systems Requirements Document, Ferrell Mercer, Bill Dalton & Mike Richards, Version 2.05, [redacted].	SRD-DMR-1-6/11/99
VersaMax Phase 2 IC200CPU005, S. Hogge & D. McComsey, Version 2.0, [redacted]	MFR_SAH_1_05181999
Requirements for 90-30 Model 364 Support for Transactional Datagrams and PPP, Ferrell Mercer, in draft	N/A
General Ethernet & PLC-related reference documents:	
TCP/IP Ethernet Communications for the Series 90 PLC – Station Manager Manual, GFK-1186F	GFK-1186F
Series 90™-30 Programmable Controllers Installation and Hardware Manual, GFK-0356P, [redacted]	GFK-0356P
Series 90™ PLC Serial Communications User's Manual, GFK-0582C, [redacted]	GFK-0582C
Series 90™-30/90-20 Programmable Controllers Reference Manual, GFK-0467L, [redacted]	GFK-0467L
Mentor Design Database Path: /home/s9030/comm/e35a1/e35a1_f0_r00	N/A
This Document's Location Path: \\chopdsrv2\Shared\90-30\Data\cpu374\Design Documents\product designs\Hardware\e35a1\board spec\E35A1_Hardware_Description_r0.60.doc	44A747987
CPU374 eNoteBook http://gein-pd.cho.ge.com/hwweb/enotebooks/	BRDDESC-xxx-xxxxxx

Table 2-1 Applicable Documents

3 ABBREVIATIONS

Also refer to the list of terms in the CPU374 SRD (ref.2).

ASIC	Application Specific Integrated Circuit
API	Application Programming Interface
CPU	Central Processing Unit - Used as term for main system controller module.
CAN	Controller Area Network
Data rate	The rate at which the physical transfer of data (bits, bytes, words ...) occurs between any two devices within a system. The units may vary and must be specified (i.e. bits per seconds, megabytes per second ...)
Field Units	All components of the *VersaMax* intended to be installed at the process under control - basically all devices except the programmer.
Goal	Desirable feature, quality, or quantity of an item. Differs from a requirement in that achieving the goal during the design phase is highly desired as opposed to required.
HMI	Human Machine Interface
NIU	Network Interface Unit. The field bus slave interface allowing the VersaMax IO connected to that IO.
RDS	Reliable Data Service, a protocol above UDP that provides a subset of the data transfer reliability of TCP.
RTC	Real Time Clock. Special timer within the CPU used to schedule events in the firmware. This clock does not keep track of the real world time and date. See TOD Clock.
RTU	Remote Terminal Unit
SNP	Series Ninety Protocol
SRTP	Service Request Transfer Protocol
Sweep impact	The amount of time added or removed from the complete execution loop of the CPU / NIU by the item in question. The item can be hardware, firmware, or software.
Target	Specified value of a goal. (ie. Should be smaller than 70mm ...).
TCP	Transmission Control Protocol, a connection-oriented reliable data transfer protocol.
TOD Clock	Time-Of-Day Clock. Special device and/or software designed to keep track of the real world time and date.
UDP	User Datagram Protocol, a connectionless non-reliable data transfer protocol.
MFR	Marketing Functional Requirement
PFR	Product Functional Requirement
CTQ	Critical to Quality
NDC	Net Distributor Cost
OEM	Original Equipment Manufacturer
TVC	Total variable cost
SRTP	Service Request Transfer Protocol
EGD	Ethernet Global Data
UDP	User Datagram Protocol
IGMP	Internet Group Management Protocol

4 HARDWARE DESCRIPTION

The hardware for the 90-30 CPU 374 consists of two separate components, the CPU hardware and the Ethernet hardware. The CPU hardware design is a new motherboard design using AMD SC520 processor.(CY3A1). The Ethernet hardware is a daughterboard design which will interface directly to SC520 motherboard using a slightly different electrical and mechanical interface as the CPU364 design dictates today. Refer to *5.3(Motherboard Connector Diagram)* & *CPU360 Daughterboard Interface Specification*. This hardware description document is limited to the Ethernet hardware board only, this board will henceforth be referred to as the "E35A1".

4.1 BLOCK DIAGRAM

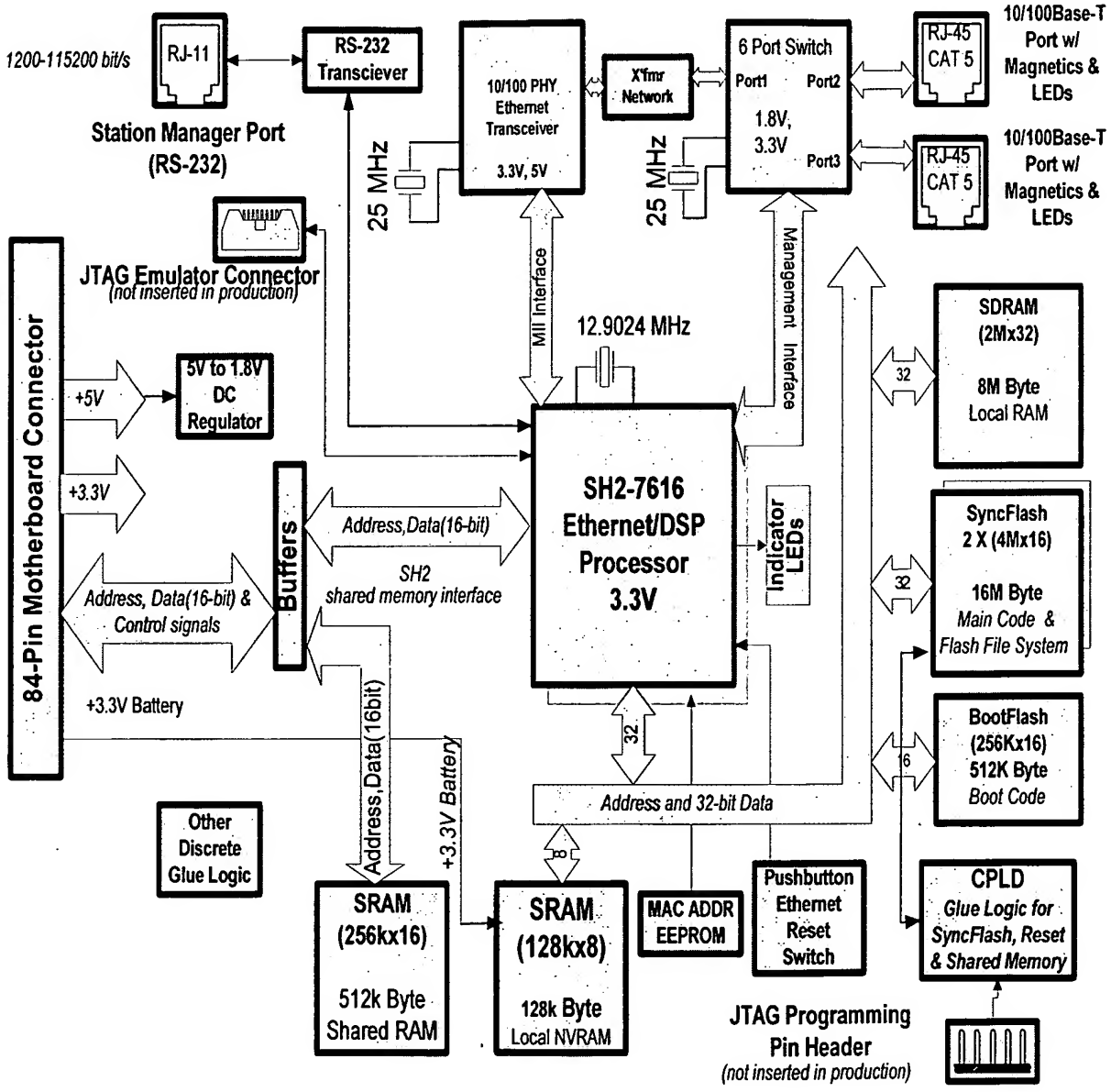

Figure 4-1 E35A1 Daughterboard w/Serial Port & 10/100base-T Ethernet (Block Diagram)

4.2 90-30 CPU374 Feature Comparison with 90-30 CPU364 & VersaMax CPUE05

Category	90-30 CPU364	VersaMax CPUE05	90-30 CPU374
Ethernet Interface	AAUI and base-T (AAUI & RJ45) Half-duplex only	base-T/base-TX only (RJ45) Full/Half-duplex, autoselect	base-T/base-TX only (RJ45) Full/Half-duplex, autoselect
Interface Speed	10-Mbits/sec (10base-T)	10- or 100-Mbits/sec 10base-T / 100base-TX (autodetect / autoswitch)	10- or 100-Mbits/sec 10base-T / 100base-TX (autodetect / autoswitch)
Operating System	GEF Proprietary	pSOS	VxWorks
Processor	Intel i386EX	NetSilicon Net+ARM/40	Hitachi SH2-7616
Core Frequency	25 MHz	25 MHz	51.6 MHz
Memories: RAM Flash Non-Volatile RAM	 1MB SRAM 1MB + 128kB (boot) (all RAM above)	 1MB SRAM 4MB 128Kb	 8MB SDRAM 512KB (boot) + 16 MB SyncFlh is partitioned: F/w & Flash File System 128kB
DB Interface	64kB Shared RAM	64kB (ENI Interface)	512KB Shared RAM
MAC Address	Programmed into Flash at Final Test	Serial EEPROM 4Kbit, programmed at Final Test	Serial EEPROM 4Kbit, programmed at Final Test
Station Manager Port	Dedicated RS-232 (6-pin RJ-11 jack)	Shared RS-232 (mux with CPU) 9-pin DSUB female conn.	Dedicated RS-232 (6-pin RJ-11 jack)
LEDs	3 Single Color LEDs (Green) (EOK, LAN, STAT)	3 Bi-color LEDs (Green/Amber) (LAN, STAT, PORT 1)	3 Single Color LEDs (Green) (EOK, LAN, STAT)
ENet Side Core Voltage	+5.0VDC	+3.3VDC	+3.3VDC
TVC	$400 (from SAP [redacted])	$350 (est.)	$209 (est.) (For E35A1) $241 (est.) (For CY3A1)

Table 4-1 Main hardware differences between CPU364, CPU374, and VersaMax CPUE05

4.3 ETHERNET HARDWARE

4.4 PROCESSOR

The Ethernet hardware is based on SH2 7616 processor, which has the following features:

32-bit RISC processor
32-bit internal and external Data bus
25-bit address bus
30-bits of General Purpose I/O
Five (5) Programmable chip selects
Selection for 32/16/8-bit data bus mode
Normal and Burst operation
Glueless Flash, SRAM, and SDRAM interface
1 Watchdog Timer
5 External & 10 Internal Interrupts
4K Cache memory
Dedicated DMA support
2 Serial Comm UARTs
10/100Mbit Media Access Controller MII Interface to external Ethernet PHY
208-pin TQFP (20-mil pitch) package

Refer to the SH2 7616 Hardware Reference Manual for additional information.

4.5 PROCESSOR CLOCKS

The processor will use a 12.9024 MHz crystal to generate the following clocks:
Ø (System Clock), EØ (External Interface Clock), IØ (CPU core clock), PØ (Peripheral clock).
Ø is the clock source for the Watchdog Timer, EØ is the clock source for SyncFlash, SDRAM and CPLD, IØ is the clock source for CPU core, PØ is the clock source for Auto Refresh for SDRAM, Baud Rate Generator. Factors affecting the selection of the frequency included the maximum clock frequency the SyncFlash could support, and also to obtain a correct divisible value to generate Baud Rates with 0% Error on the Baud Rate Generator. The external mode pins determine the initial state of the on-chip oscillator. These pins are setup for mode 0 ("000"). In this mode, PLL circuit 1 and PLL circuit 2 are initialized to the on state by a power-on reset. (Pins MD2, MD1, MD0 = 000 & CKPREQ_/CKM =1), and Frequency Modification Register (FMR) (FMR register: FR3,FR2,FR1,FR0 = 1110,which sets EØ=IØ=4*Fxtal, PØ=2*Fxtal), also we will operate with both PLL1 and PLL2 enabled, hence Frequency Modification Register (FMR.PLL1ST =0 & FMR.PLL2ST =0).

Clock	Max Frequency (MHz)	Frequency Controlled By	Components
Ø (System Clock)	51.6096	Ø = 4*Fxtal (Fxtal = 12.9024 MHz)	Watchdog Timer
EØ (External Interface Clock)	51.6096	EØ = 4*Fxtal (Fxtal = 12.9024 MHz)	SyncFlash, SDRAM, CPLD
IØ (CPU core clock)	51.6096	IØ = 4*Fxtal (Fxtal = 12.9024 MHz)	CPU Core
PØ (Peripheral clock)	25.8048	PØ = 2*Fxtal (Fxtal = 12.9024 MHz)	SDRAM Auto Refresh, Baud Rate Generator

Table 4-2 SH7616 Clock Settings

4.6 CHIP SELECTS

SH7616 has 5 Chipselects, and a maximum of 32 Mbytes for each of the address spaces CS0 to CS4 can be accessed. Memory type (DRAM, synchronous DRAM, burst ROM, etc.) can be specified for each space. Bus width (8, 16, or 32 bits) & software wait state insertion can be selected for each space. Each Chip select has a dedicated external Wait signal input. Also, there are individual WE3_ - WE0_ write signals for each byte of the 32 bit data bus.

Chip Select	Signal Name	Destination	Description
CS0_	FLHCS_	FLASH	Boot FLASH 1
CS1_	SR2CS_	NV SRAM	Battery Backed SRAM
CS2_	SYNCFCS_	SYNCFLASH	System Primary FLASH & FLASH File System
CS3_	SDRCS_	SDRAM	System SDRAM (Data)
CS4_	SR1CS_	Shared Memory	Shared SRAM

Table 4-3 SH7616 Chip Select Assignments

4.7 TIMERS

The SH7616 has three 16-bit timer channels in its TPU (Timer Pulse Unit). The timers operate using the Peripheral clock (PØ) or external clocks. Refer to the TPU section in the SH2 7616 Hardware Reference Manual for programming details.

4.8 WATCHDOG TIMER

A single-channel watchdog timer (WDT) is provided on-chip for monitoring system operations. If a system becomes uncontrolled and the timer counter overflows without being rewritten correctly by the CPU, an overflow signal (WDTOVF_) is output externally. This overflow signal (WDTOVF_) is used to reset the Processor and the Peripherals. (BootFlash, SyncFlash). The WDT should also generate an internal reset signal for the entire chip. The watchdog timer control/status register (WTCSR) should be configured to enable a Reset after the timer has overflowed.
The following table can be used to calculate the reset timeout period with the Crystal clock = 12.9024 MHz.

Watchdog Timer Control Register, CKS2-0 bits	Formula Ø=4*Fxtal =4*12.9024 = 51.6096 MHz	Timeout Period (msec)
000	Ø/4	0.0197
001	Ø/128	0.6324
010	Ø/256	1.2648
011	Ø/512	2.5298
100	Ø/1024	5.0595
101	Ø/2048	10.1190
110	Ø/8192	40.4761
111	Ø/16384	80.9524

Table 4-4 SH7616 Watchdog Timeout Periods (Xtal = 12.9024 MHz)

4.9 DMA CHANNELS

The SH7616 contains 2 DMA channels for moving data between external devices and internal peripherals with minimal CPU intervention. Both channels support memory to memory operations. The SH7616 also has an on-chip two-channel Ethernet direct memory access controller (E-DMAC) directly connected to the Ethernet controller (EtherC). A large proportion of buffer management is controlled by the E-DMAC itself using descriptors.This lightens the load on the CPU and enables efficient data transfer control to be achieved. It achieves efficient system bus utilization through the use of block transfer (16-byte units) and supports single-frame/multi-buffer operation. The E-DMAC cannot handle transfers to on-chip RAM and supporting modules.

4.10 INTERRUPTS

The SH7616 contains 4 external interrupts, and a NMI (Non-Maskable Interrupt) input. The external Interrupt inputs can be programmed to be either in IRL mode or IRQ mode. In IRQ mode, each of signals IRL3 to IRL0 functions as a separate interrupt source. In IRL mode, these signals can specify interrupt priority levels 1 to 15. On the E35A1 board we will use the IRQ mode.
An IRQ interrupt is requested when the external interrupt vector mode select bit (EXIMD) of the interrupt control register (ICR) is set to 1. An IRQ interrupt corresponds to input at one of pins IRL3_ to IRL0_. Low-level sensing or rising/falling/both-edge sensing can be selected independently for each pin by the IRQ sense select bits (IRQ00S–IRQ31S) in the IRQ control/status register (IRQCSR), and a priority level of 0 to 15 can be selected independently for each pin by means of interrupt priority register C (IPRC).

Interrupt	Signal Name	Description	Trigger Level/Edge
IRQ0_	MII_IRQ_	Configurable interrupt request from Ethernet PHY	Falling Edge
IRQ1_	PBINT	Pushbutton input to request Ethernet Reset ('1' = Switch is activated)	Rising Edge
IRQ2_	SR_MB_INT	Interrupt from the SC520 Motherboard	Rising Edge
IRQ3_	Spare	Unused	-
NMI	ACFAIL	Interrupt from the SC520 Motherboard	Rising Edge

Table 4-5 SH7616 Interrupt Descriptions

4.11 PROCESSOR PORTS

The SH7616 contains two I/O ports, Port A is a 14-bit input/output port, and port B is a 16-bit input/output port. The port pins are multiplexed as general input/output and other functions. (The function of multiplexed pins is selected by the pin function controller (PFC)). Each pin can be configured as general purpose I/O or serial channel or interrupt signals.

SH7616 Port Pin	I/O 'Initial Value'	Signal	Description
PA13 / SRCK0	I	PBINT	Reset Pushbutton Input ('1' = Button Active)
PA12 / SRS0	I	BOOT_LD	Force Ethernet board to boot mode
PA11 / SRXD0	O '0'	LED_STATUS	Ethernet STAT LED Control
PA10 / STCK0	O '0'	LED_OK	Ethernet Board OK
PA9 / STS0	O '0'	LED_LAN1	Ethernet LAN LED Control 1
PA8 / STXD0	O '0'	LED_LAN2	Ethernet LAN LED Control 2
PA7 / **WDTOVF_**	O '0'	WDT_RESET_OUT_	Watchdog Reset Output
PA6 / FTCI	I	SDA	EEPROM Data
PA5 / FTI	O '0'	SCL	EEPROM Clock
PA4 / FTOA	O '1'	SR_DB_INT	Shared RAM Interrupt
PA2 / LNKSTA	O '0'	RESET_OUT_	Reset Output
PA1 / EXOUT	O '1'	EEPRM_RST	EEPROM Reset
PA0	I	Spare	Not Used

SH7616 Port Pin	I/O 'Initial Value'	Signal	Description
PB15/SCK1	I	Spare	Not Used
PB14/**RXD1**	I	RXD1	Receive Input
PB13/**TXD1**	O	TXD1	Transmit
PB12/SRCK2/RTS_/STATS1	O	RTS_	Request to Send
PB11/SRS2/CTS_/STATS0	I	CTS_	Clear to Send
PB10/SRXD2/TIOCA1	I	FW_ID2	Firmware ID '000' to '011' for CPU374 '100' to '111' for ENIU (4 versions possible for each) '000' & '111' are the initial versions resp. for CPU374 & ENIU.
PB9/STCK2/TIOCB1/TCLKC	I	FW_ID1	
PB8/STS2/TIOCA2	I	FW_ID0	
PB7/ STXD2/TIOCB2/TCLKD	O '1'	SMP_SCK	Switch Management Port Clock
PB6/SRCK1/SCK2	O '1'	SMP_SS_	Switch Management Port Enable
PB5/SRS1/RXD2	O '1'	SMP_MOSI	Data Out from the Switch Management Port
PB4/SRXD1/TXD2	I	SMP_MISO	Data In to the Switch Management Port
PB3/ STCK1/TIOCA0	NA	Not Used	Non-functional (Needs Bug fix on the Chip)
PB2/ STS1/TIOCB0	NA	Not used	Non-functional (Needs Bug fix on the Chip)
PB1/ STXD1/TIOCC0/TCLKA	O '0'	LED_SELECT	Ethernet Connector LEDs control select
PB0/ TIOCD0/TCLKB/WOL	O '0'	LED_ON	Ethernet Connector LEDs On/Off

Table 4-6 SH7616 Port Pin Assignments

4.12 UART's

The SH7616 is equipped with a two-channel serial communication interface with built-in FIFO buffers (SCIF). The SCIF can handle both asynchronous and synchronous serial communication. The E35A1 will only use one of these channels to run the RS-232 port (6-pin RJ 11). The E35A1 will use this port to support station manager. **On the E35B1 board, this feature is not supported, thus the RS-232 port RJ 11connector will not be populated.**

Processor Pin	I/O	Signal	Description
PB14/**RXD1**	I	RXD1	Receive Input
PB13/**TXD1**	O	TXD1	Transmit
PB12/SRCK2/RTS_/STATS1	O	RTS_	Request to Send
PB11/SRS2/CTS_/STATS0	I	CTS_	Clear to Send

The bit-rate generator for each port will use the internal Peripheral clock Pclk = 25.8048 MHz. The serial control register (SCSCR) should be configured to accept an internal clock source. (SCSCR.CKE[1:0]=01).
The following table shows the baud rates supported by the SH2. Using 16 bit mode with Pclk as input to BRG. (operating on a base clock which is 16 times bitrate), N=(Pclk/2*Fbrg*16)-1
SCBRR settings = Values of 'N', where 'N' is a 8 bit register, thus possible values range from 0 to 255.
SCSMR settings = Values for SCSMR.CKS[1:0] - Refer Table Below.

Bit Rate	n	SCSMR.CKS[1:0]	SCBRR (N)	% Error
1200	1	[01]	167	0%
2400	1	[01]	83	0%
4800	0	[00]	167	0%
9600	0	[00]	83	0%
19200	0	[00]	41	0%
38400	0	[00]	20	0%
57600	0	[00]	13	0%
115200	0	[00]	6	0%

Table 4-7 SH7616 RS-232 Signal Assignments

4.13 MAC ADDRESS

The E35A1 will contain a unique identification number called the MAC address. This 12 digit hexadecimal number provides a unique identification number to an Ethernet node. It will be programmed into a 4K serial EEPROM, which is connected to the SH7616 through general purpose ports. The port pin PA1 (EEPRM_RST), is used to control the EEPROM reset. This is a active high signal and EEPRM_RST = 1 will reset the EEPROM. For programming details, refer to the 24C04 datasheet.

4.14 MEMORY

Overview:

Type	Size	Speed	Organization
Flash (Boot)	512 Kbyte	100ns 6-state read 6-state writes	256K x 16
SyncFlash (Primary Flash & Flash File System)	16 Mbyte	9ns CAS latency = 2, Trcd = 2, for Burst Read & Normal Write	4Mbit x 32
SDRAM	8 Mbyte	7 nsec CAS latency = 2, Trcd = 2, for Burst Read & Normal Write	2Mbit x 32
Battery Backed SRAM	128 Kbyte	100ns 6-state reads 6-state writes	128K x 8
Shared SRAM	512 Kbyte	15 nsec 3-state reads 3-state writes	256K x 16
Internal Cache	4 Kbyte		

Table 4-8 SH7616 Memory Settings

4.14.1 CACHE

SH7616 incorporates 4 kbytes of four-way,mixed instruction/data type cache memory. The cache is arranged in a 4-way set associative configuration . Each cache-set can be configured to cache instructions, data, or both. It can also be configured to be used as a 2Kbyte block of cache and a 2Kbyte block of RAM. Refer to section 8.1 in the SH2 7616 Hardware Reference Manual for more details.

4.14.2 BOOT FLASH

The SH7616 will have 512 KB of Flash memory organized as 256Kx16-Bit device. It will store the boot loader. Read & Writes to this Boot Flash take 6 clock cycles. Refer to Timing Analysis Read, Writes for details.
Wait state register should be configured with 4 wait states, also 1 idle cycles should be between consecutive read or write accesses, since the FLASH is slow in turning off its data buffers. In order to write to a sector, a command sequence must be written to the Flash. The command sequences are located in the datasheet and the addresses for the commands should be shifted to the left by one bit (the lower address line from the SH7616 is not attached to the Flash). Refer to the Am29LV400B Data sheet for more details. Refer to the following table, for programming register details.

Register	Bits	Value	Description
BCR1(Bus Control Register 1)	BSTROM	0	Not a Burst ROM
BCR1(Bus Control Register 1)	A0LW1,A0LW0	01	Wait cycles = 4
BCR3(Bus Control Register 3)	A0LW2	0	Wait cycles = 4
WCR1(Wait Control Register 1)	IW01,IW00	01	Idle cycles = 1
WCR2(Wait Control Register 2)	A0WM	1	External Wait Input Ignored
WCR3(Wait Control Register 3)	A0SHW1, A0SHW0	01	CS_ assert period extension

Table 4-9 Boot Flash Memory Register Settings

4.14.3 SHARED MEMORY

The SH7616 will communicate with the SC520 Motherboard through 512k byte of shared RAM. The shared RAM is a 15 nsec SRAM arranged as 256k x 16, all of which will be addressable, by the SH7616. A Xilinx PLD is programmed with the arbitration logic when both SC520 and SH7616 want to access the SRAM, one of them gets the control and the other is indicated to wait by the Ready/Busy control signal. During the accesses to the shared memory, the SH7616 can send an interrupt to SC520 (Port pin PA4 - SR_DB_INT) or can receive an interrupt from SC520 (IRQ2_ - MB_INT). Refer to Timing Analysis Shared SRAM Read/Write, for details.
2 idle cycles should be inserted between consecutive read or write accesses, also WCR3 should be programmed to have CS_ assert period extension.

Register	Bits	Value	Description
BCR1(Bus Control Register 1)	A4ENDIAN	0	Big Endian
BCR2(Bus Control Register 2)	A4SZ1, A4SZ0	10	Data width = 16 bit
WCR2(Wait Control Register 2)	A4WD1,A4WD0	00	1 cycle wait from 'Wait' negation to 'RD/WR' negation
WCR2(Wait Control Register 2)	W41, W40	01	External Wait Input Enabled with '1' software wait states
WCR2(Wait Control Register 2)	IW41,IW40	10	Idle cycles = 2
WCR2(Wait Control Register 2)	A4WM	0	External Wait Input Enabled
WCR3(Wait Control Register 3)	A4SW2, A4SW1,A4SW0	000	CS_ assert period extension
WCR3(Wait Control Register 3)	A4HW1, A4HW0	00	CS_ assert period extension

Table 4-10 Shared Memory Register Settings

4.14.4 SDRAM

The E35A1 will have 8Mbyte of SDRAM memory arranged as 4 banks of 512 Kbit each and with 32 bit data bus. (512 K x 4 x 32). This RAM memory is used for volatile storage and it is not backed up on the power cycles. The SDRAM initialization requires at least 100 usecs after reset before any accesses or commands are issued to the SDRAM device, and configuration is done in a predefined manner with specific sequence of commands being issued to the SDRAM.(COMMAND INHIBIT, PRECHARGE etc).Refer the SDRAM Datasheet for more details. For both Read and Writes the CAS latency should be set to '2', and '2' idle cycles should be inserted between consecutive accesses, Trcd should be configured for 2 states. A maximum Burst length = '4', is possible with data

width = 32 bit. Refer to Timing Analysis SDRAM Read/Write, for details. For Auto Refresh the SDRAM requires 4,096 AUTO REFRESH cycles every 64 msec. Refer to the following table, for programming register details.

Register	Bits	Value	Description
WCR1(Wait Control Register 1)	W31,W30	01	CAS latency = 2
WCR1(Wait Control Register 1)	IW31,IW30	10	Idle cycles = 2
MCR(Memory Control Register)	RCD1,RCD0	01	Trcd = 2 cycles (Between ACTIVE & READ)
MCR(Memory Control Register)	TRP1,TRP0	00	Trp= 1cycles (Between PRECHARGE & ACTIVE)
MCR(Memory Control Register)	TRWL1,TRWL0	00	Tras = 1 cycles (Write PRECHARGE Delay)
MCR(Memory Control Register)	RASD	0	AUTO-PRECHARGE followed by BANK ACTIVE
MCR(Memory Control Register)	TRAS1,TRAS0	00	Trfc = 3cycles (AUTO REFRESH Period)
MCR(Memory Control Register)	AMX2,AMX1,AMX0	000	64 Mbit SDRAM
MCR(Memory Control Register)	SZ	1	LongWord (32-bit)
MCR(Memory Control Register)	RFSH,RMODE	10	Auto Refresh
BCR1(Bus Control Register 1)	A2ENDIAN	0	Big Endian
BCR1(Bus Control Register 1)	DRAM2 - DRAM0	101	SDRAM
BCR2(Bus Control Register 2)	BASEL	0	4 Banks
BCR2(Bus Control Register 2)	BWE	0	Burst Write Disabled
RTCSR(Refresh Timer Control)	CKS2 - CKS0	001	(PØ/4 = 25.8048 MHZ/4) is the refresh clock source
RTCSR(Refresh Timer Control)	RRC2 - RRC0	100	8 Refreshes
RTCNT(Refresh Timer Counter)	RTCNT7 - RTCNT0	01100100	To obtain 4096 refresh cycles Every 64 msec, at a frequency of 8 refreshes every 15.6 µsec

Table 4-11 SDRAM Memory Register Settings

4.14.5 BATTERY BACKED SRAM

To meet the need for Non-volatile memory of the SH7616, battery backed SRAM is included on the board. The SRAM has an access time of a 100nS and is organized in a 128Kx8-Bit device. The SH7616 will be able to access the memory with a 6-state cycle (4 wait states) for Reads and Writes.
Refer to Timing Analysis NVRAM Read/Write, for details. Wait state register should be configured with 4 wait states, also 2 idle cycles should be inserted between consecutive read or write accesses, since the NVRAM is slow in turning off its data buffers. Refer to the NVRAM Data sheet for more details. Refer to following table for programming register details.
On the E35B1 board, the Battery Backed Memory feature is not supported, thus the SRAM alongwith it's associated circuitry will not be populated.

Register	Bits	Value	Description
BCR1(Bus Control Register 1)	A1LW1,A1LW0	01	Wait cycles = 4
BCR2(Bus Control Register 2)	A1SZ1, A1SZ0	01	Data width = 8 bit
BCR3(Bus Control Register 3)	A1LW2	0	Wait cycles = 4
WCR1(Wait Control Register 1)	IW11,IW10	10	Idle cycles = 2
WCR2(Wait Control Register 2)	A1WM	1	External Wait Input Ignored
WCR3(Wait Control Register 3)	A1SHW1, A1SHW0	01	CS_ assert period extension

Table 4-12 NVRAM Memory Register Settings

4.14.6 SYNC FLASH (PRIMARY FLASH & FLASH FILE SYSTEM)

The SH7616 will have 16MB of Sync Flash memory organized as two 4Mx16-Bit devices connected to realize a 4Mx32-Bit device. This memory will store the Primary Firmware, User Program, Ethernet Toolkit Application, and the Flash File System. The firmware has control over the location and sizes of all these components. Refer to Firmware design document (xxx-xxx) for more details on Flash File System, Ethernet Toolkit Application. The Sync Flash device is a nonvolatile, electrically sector-erasable (FLASH), programmable memory having a SDRAM Read/Write Interface. It is a fully synchronous device, with signals getting registered on the rising edge of the clock.. It has a four bank, uniform sector architecture. Burst Read accesses with programmable Burst lengths are possible, thus allowing higher data rates, Write accesses are single location. The SyncFlash initialization requires at least 100 usecs after reset before any accesses or commands are issued to the device, and configuration is done in a predefined manner with specific sequence of commands being issued to the SyncFlash.(LOAD COMMAND REGISTER, ACTIVE, READ/WRITE etc.).Refer the Sync Flash Datasheet for more details. Also, refer Interfacing-to-SyncFlash Application note for details on roles of Boot device and CPLD.

Role of the Boot Flash :
To have the SyncFlash be used for primary firmware, some start-up code should be provided in ChipSelect 0 area. This start-up code will implement a minimal boot, to initialize the SyncFlash device and configure the SH7616 for synchronous memory operation before jumping to SyncFlash memory and continuing the boot process. To accomplish this, the Boot Flash is programmed to provide the following functions before jumping to SyncFlash memory :
1. An initial 100µs delay loop must be implemented to enable the SyncFlash device to power-up after a reset.
2. Areas 2 and 3 must be configured for SDRAM operation.
3. Areas 2 and 3 must be configured for 32-bit-wide operation.
4. The CAS latency must be set to '2' cycles.
5. The t RC (RAS-to-CAS time) must be set to '2' cycles.

Role of the CPLD :
1) To prevent REFRESH commands from reaching Sync Flash.
2) To issue a LCR command sequence for Read/Write accesses.

SH7616 has a common programming register set for Chip Select 2 & Chip Select 3 areas, which are both programmed for SDRAM interface, but since Chip Select 2 is SyncFlash & Chip Select 3 is SDRAM, the standard SDRAM command set needs to be modified somewhat to provide complete SyncFlash functionality. When refresh is enabled for SDRAM operation, areas 2 and 3 simultaneously receive the REFRESH operation. Because an SDRAM REFRESH command is redefined as a LOAD COMMAND REGISTER (LCR) command on a SyncFlash device, REFRESH operations must be prevented from reaching the SyncFlash device; otherwise, a REFRESH command could be misinterpreted by the SyncFlash device and start an unexpected LCR sequence. Also, the CPLD has to perform a command transform to issue a LCR sequence to the SyncFlash for Read/Write accesses.

For both Read and Writes the CAS latency should be set to '2', and '2' idle cycles should be inserted between consecutive accesses, Trcd should be configured for 2 states. A maximum Burst length = '4', is possible with data width = 32 bit. Refer to Timing Analysis SyncFlash Read, Write, for details.

Register	Bits	Value	Description
WCR1(Wait Control Register 1)	W31,W30	01	CAS latency = 2
WCR1(Wait Control Register 1)	IW31,IW30	10	Idle cycles = 2
MCR(Memory Control Register)	RCD1,RCD0	01	Trcd = 2 cycles (Between ACTIVE & READ)
MCR(Memory Control Register)	AMX2,AMX1,AMX0	000	128 Mbit SyncFlash
MCR(Memory Control Register)	SZ	1	LongWord (32-bit)
BCR1(Bus Control Register 1)	A2ENDIAN	0	Big Endian
BCR1(Bus Control Register 1)	DRAM2 - DRAM0	101	SDRAM Interface
BCR2(Bus Control Register 2)	BASEL	0	4 Banks
BCR2(Bus Control Register 2)	BWE	0	Burst Write Disabled

Table 4-13 SyncFlash Memory Register Settings

4.15 MEMORY MAP

Below is the memory mapping details.

Type	Chip Select	Address Map
Boot Flash	CS0_	H'00000000–H'01FFFFFF
NVRAM	CS1_	H'02000000–H'03FFFFFF
Sync Flash	CS2_	H'04000000–H'05FFFFFF
SDRAM (Data)	CS3_	H'06000000–H'07FFFFFF
Shared SRAM	CS4_	H'08000000–H'09FFFFFF

Table 4-14 Memory Map

4.16 ETHERNET TRANSCEIVER (PHY)

The SH7616 supports a standard Media Independent Interface (MII) to the Ethernet transceiver (PHY). The E35A1 uses a Cirrus Logic CS8952 transceiver for it's interface to the LAN. The CS8952 provides a physical interface fully compatible with the IEEE 802.3 standard. It can be configured for either 10BASE-T or 100BASE-TX communications. Programming is accomplished through the MII interface. Refer to the CS89592 data sheet and the SH2 7616 Hardware Reference Manual (section 9) for programming details.
Also, refer to Timing Analysis.

4.17 ETHERNET SWITCH

The E35A1 has a six port 10/100 Mbps integrated switch controller, only three out of the six ports are utilized on this board. The switch has a 1Mbit on-chip packet buffer, five integrated 10/100BASE-T/TX IEEE 802.3u compliant transceivers, and MACs, and integrated address management. It supports a Serial Management Port (SMP), this port allows configuration and control of Auto-Negotiation registers. Refer to the BCM5315 data sheet for details on Serial Management Port programming.

4.18 ETHERNET LED'S

The E35A1 will contain 7 LED's to indicate Ethernet activity and status. Three LEDs (LAN, STAT, OK) are controlled by IO ports on the SH7616 and discrete logic. These LEDs are on the front faceplate of the CPU374 module. The other four LEDs are 2 pairs of green color LEDs . ('LINK/ACT', '100'). These LEDs are on the two RJ45 Ethernet connectors. These are controlled by IO ports on the SH7616 and a Multiplexer.
On the E35B1 board, the STAT LED is named FAULT LED, and its color is YELLOW instead of GREEN.

	COLOR	SH7616 Ports PA9	PA8	Resulting Function
LAN LED	Green	0	0	Green LED is off
		0	1	Green LED is on
		1	0	Reserved
		1	1	Green LED is controlled by Ethernet PHY transmission activity.

Table 4-15 LAN LED Description

	COLOR	SH7616 PA11	Resulting Function
STAT LED/ FAULT-LED(On E35B1)	Green / Yellow	0	Green/Yellow LED is off
		1	Green/Yellow LED is on

Table 4-16 STAT LED Description

	COLOR	SH7616 PA10	Resulting Function
OK LED	Green	0	Green LED is off
		1	Green LED is on

Table 4-17 OK LED Description

	COLOR	SH7616 Ports PB3	PB2	Resulting Function
LINK/ACT LED	Green	0	0	Green LED is off
		0	1	Green LED is on
		1	0	Green LED is controlled by Ethernet Switch device transmission activity
		1	1	Green LED is controlled by Ethernet Switch device transmission activity

Table 4-18 LINK/ACT LED Description for Ethernet Ports 1& 2

'100' LED	COLOR	SH7616 Ports PB3	PB2	Resulting Function

	Green	0	0	Green LED is off
		0	1	Green LED is on
		1	0	Green LED is controlled by Ethernet Switch device Speed (10Mbit/100Mbit)
		1	1	Green LED is controlled by Ethernet Switch device Speed (10Mbit/100Mbit)

Table 4-19 '100' (Speed) LED Description for Ethernet Ports 1 & 2

4.19 PUSHBUTTON SWITCH

The E35A1 has a pushbutton switch used to interrupt the Ethernet interface. The switch uses a debounce filter to eliminate noise caused by the mechanical switch. The resulting signal is sent to a general purpose port and an interrupt on the SH7616. The firmware has control on how to use the switch.
On the E35B1 board, this feature is not supported, thus the switch alongwith it's associated circuitry will not be populated.

4.20 RESET

The diagram below details the reset hierarchy for the SH7616. The arrows indicate the direction of the reset signal. The SC520, the SH7616 and the reset pushbutton can all initiate a reset.
The SC520 will initiate a reset during a watchdog timeout, if it receives a reset input, or through a firmware decision. If the SC520 is reset, it will reset SH7616. The SH7616 will initiate a reset during a watchdog timeout, if it receives a reset input, or through a firmware decision. The SH7616 has a port output that will act as its reset output (PA2 Reset Output), in addition it also has a Watchdog timeout output (PA7 / WDTOVF) which gets driven on Watchdog timeout. The reset pushbutton will send a signal to an interrupt on the SH7616. The firmware has control over the use of the pushbutton. The Boot Flash and the Sync Flash are reset on a Watchdog reset or a Motherboard reset input. The PHY and the Ethernet switch are reset by the SH2 reset output.
The SC520 motherboard generates 2 resets for the E35 daughterboard, a soft reset (MB_MANUAL_RESET_), And a power up reset(MB_POWER_RESET). Either of these, resets the E35 daughterboard with the exception for the Shared RAM interface, the Shared RAM interface only gets reset on a power up. (MB_POWER_RESET).

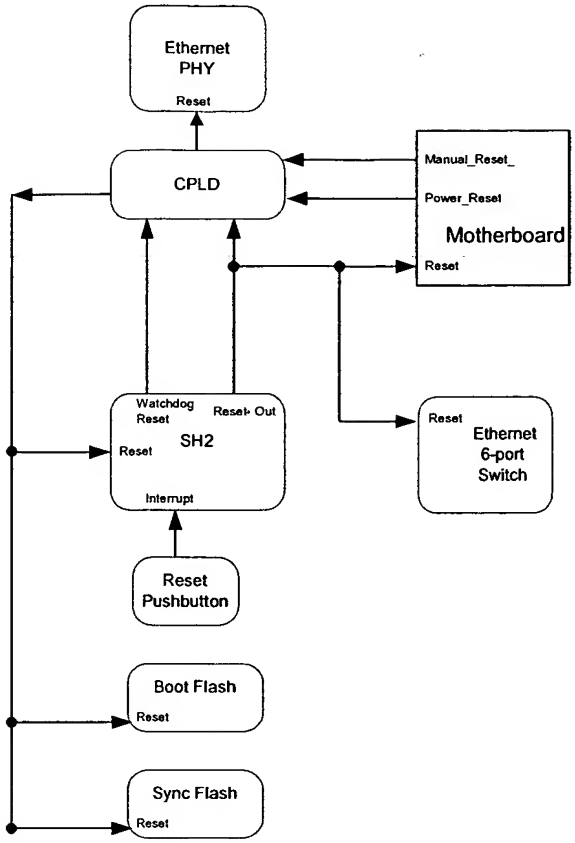

Figure 4-2 Reset Structure

4.21 HARDWARE INITIALIZATION & FIRMWARE TESTABILITY

4.21.1 SH7616 CONFIGURATION AT POWERUP.

Pins	Value(1: Ext Pullup, 0: Ext Pulldown)	Description
MD4,MD3	01	Chip Select 0 - 16 bit wide
MD2,MD1,MD0	000	Clock Mode 0 (PLL1 &PLL2 used)

Table 4-20 SH7616 Powerup Configuration

4.21.2 FIRMWARE TESTABILITY

A 140 pin high density connector is provided on the board for Firmware Testability. This connector will have the System Address, Data bus and Control signals. This connector will not be populated on production boards.

Pin	
71	DPA1
72	DPA2
73	DPA3
74	DPA4
75	DPA5
76	DPA6
77	DPA7
78	DPA8
79	DPA9
80	DPA10
81	DPA11

Pin	
70	
69	
68	
67	SH_WAIT_
66	
65	
64	BE1_
63	BE0_
62	SR1CS_
61	MB_DIR_
60	D31

82	DPA12	59	D30
83	DPA13	58	D29
84	DPA14	57	D28
85	DPA15	56	D27
86	DPA16	55	D26
87	DPA17	54	D25
88	DPA18	53	D24
89	SH_OE_	52	D23
90		51	D22
91	FLHCS_	50	D21
92	DPD0	49	D20
93	DPD1	48	D19
94	DPD2	47	D18
95	DPD3	46	D17
96	DPD4	45	D16
97	DPD5	44	D15
98	DPD6	43	D14
99	SDRCKE	42	D13
100	SDR_CLK	41	D12
101	DPD7	40	D11
102	DPD8	39	D10
103	DPD9	38	D9
104	DPD10	37	D8
105	DPD11	36	D7
106	DPD12	35	D6
107	DPD13	34	D5
108	DPD14	33	D4
109	DPD15	32	D3
110	SR2CS_	31	D2
111	SYNCFCS_	30	D1
112	SDRCS_	29	D0
113		28	MB_OE_
114		27	DB_DIR_
115	DP_BHE_	26	DB_OE_
116	DP_BLE_	25	A24
117	DPWE_	24	A23
118	DPOE_	23	A22
119	DPCS_	22	A21
120	DB_ADDR_OE_	21	A20
121	MB_ADDR_OE_	20	A19
122	SDRCAS_	19	A18
123	SDRRAS_	18	A17
124	SDRWE_	17	A16
125	SYNCFCAS_	16	A15
126	SYNCFRAS_	15	A14
127	SYNCFWE_	14	A13
128	PHY_RESET	13	A12
129	WDT_RESET_OUT_	12	A11
130	RESET_	11	A10
131		10	A9
132		9	A8
133	MII_IRQ_	8	A7
134	PBINT	7	A6
135		6	A5
136		5	A4
137		4	A3
138	BE3_	3	A2
139	BE2_	2	A1
140		1	A0

Table 4-21 Pinout for the Debug Connector

4.22 EXTERNAL JUMPER TO DISABLE SH7616 BOOTSTRAP FROM FLASH

At powerup, to disable SH7616 to boot-up from Flash, there is a 3 pin header provided. Refer to the figure 4-3. If the bottom 2 pins (labeled "FLH_EN") are shorted together then Flash is bootstrap enabled, if the top 2 pins (labeled "FLH_DIS") are shorted together then the Flash is disabled.

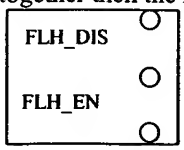

Figure 4-3 Jumper setting for SH7616 bootstrap

4.23 EXTERNAL SIGNAL TO INDICATE FORCING SH7616 TO BOOT MODE

There is a Test point provided on the board (will be labeled), to enable the E35A1 board to be forced to boot mode. It should be shorted to ground, to force the board to boot mode. (Use the screwdriver tip).This signal is provided as an input to port pin PA12 on the SH7616.

4.24 BOARD ID

The identification of CPU374 and ENIU firmware versions are accomplished by tying resistors to specific port pins on the SH7616. There are 3 port pin inputs (PB10,PB9,PB8) which provide a total of 8 possible Firmware Ids. 4 of the 8 are for CPU374 and the remaining 4 are for ENIU. The first version of CPU374 will have a firmware ID of '000' and the ENIU will have a firmware ID of '111'.

FW_ID2, FW_ID1, FW_ID0	FirmwareVersion
000	CPU374 Version 1
001	CPU374 Version 2
010	CPU374 Version 3
011	CPU374 Version 4
100	ENIU Version 4
101	ENIU Version 3
110	ENIU Version 2
111	ENIU Version 1

Table 4-22 Board ID for different firmware versions

5 INPUTS & OUTPUTS

5.1 POWER SUPPLY

The E35A1 will get its power supply from the Motherboard 82 pin connector. This connector will provide the +5VDC and +3.3VDC and Vbattery (+3.3VDC) as well as the system GND (0V) reference.

Connector Pin	Signal	Description
A4, B5, C6, D7	+5V	+5V DC
A10, B11, C12, D13	+3.3V	+3.3V DC
B2, C3, D4	0V	GND Reference
A7, B8, C9, D10	0V	GND Reference
A13, B14, C15, D16	0V	GND Reference
A17, B18, C19, D19	0V	GND Reference
A19	+3.3V	+3.3V DC Backup Battery

Table 5-1 Power Supply Pins on the Motherboard connector

5.2 RS-232 PORT CONNECTOR

The RS-232 Port connector will be a 6-pin RJ 11 connector. This port will be dedicated to the SH7616 processor. The operation of the port will be controlled by the CPU firmware.

On the E35B1 board, this feature is not supported, thus the RJ 11 connector will not be populated.

Pin	Signal	Direction	Function
1	CTS	Input	Clear to Send input
2	TXD	Output	Transmit Data output
3	GND	--	0V/Gnd signal reference
4	GND	--	0V/Gnd signal reference
5	RXD	Input	Receive Data input
6	RTS	Output	Request to Send output
7	SHLD	--	Frame GND
8	SHLD	--	Frame GND

Table 5-2 RJ 11 Connector pinout

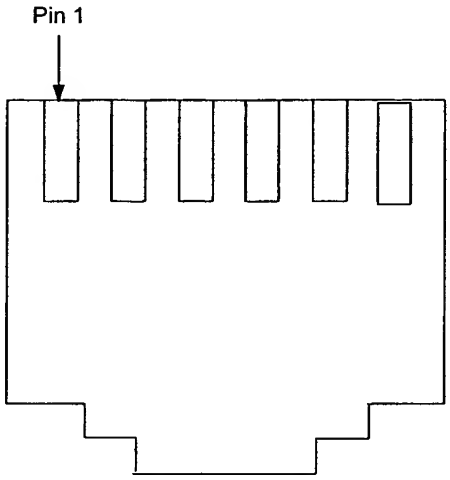

Figure 5-1 RJ 11 Connector

5.3 MOTHERBOARD CONNECTOR DIAGRAM

Note: different pinout/keying from CPU36x models!

Row:	D	C	B	A
1	0V	Spare	Spare	--KEY--
2	A1	MB_BLE_	0V	D0
3	A2	0V	D2	D1
4	0V	A3	D3	+5V
5	A5	A4	+5V	D4
6	A6	+5V	D6	D5
7	+5V	A7	D7	0V
8	A9	A8	0V	D8
9	A10	0V	D10	D9
10	0V	A11	D11	+3.3V
11	A13	A12	+3.3V	D12
12	A14	+3.3V	D14	D13
13	+3.3V	A15	D15	0V
14	MB_BHE_	A16	0V	SR_DB_INT
15	SR_MB_CS_	0V	SR_DB_RDY_	+3.3V
16	0V	MB_WR_	+3.3V	0V
17	MB_MANUAL_RESET_	+3.3V	MB_RD_	0V
18	+3.3V	A17	0V	SR_MB_INT
19	0V	0V	MB_ACFAIL	Vbatt (3.3V)
20	0V	A18	CLK33	MB_BATTCS_
21	--KEY--	RESET_OUT_	Spare	0V

Figure 5-2 Motherboard Connector

5.4 RJ45 ETHERNET CONNECTOR WITH INTEGRATED MAGNETICS & LEDS

Pin	Signal	I/O	Description
1	Tx+	O	+ Transmit output
2	Tx-	O	- Transmit output
3	RX+	I	+ Receive Input
4	FGND	-	Frame Ground
5	FGND	-	Frame Ground
6	Rx-	I	- Receive Input
7	FGND	-	Frame Ground
8	FGND	-	Frame Ground

Table 5-3 RJ-45 Ethernet Pinout

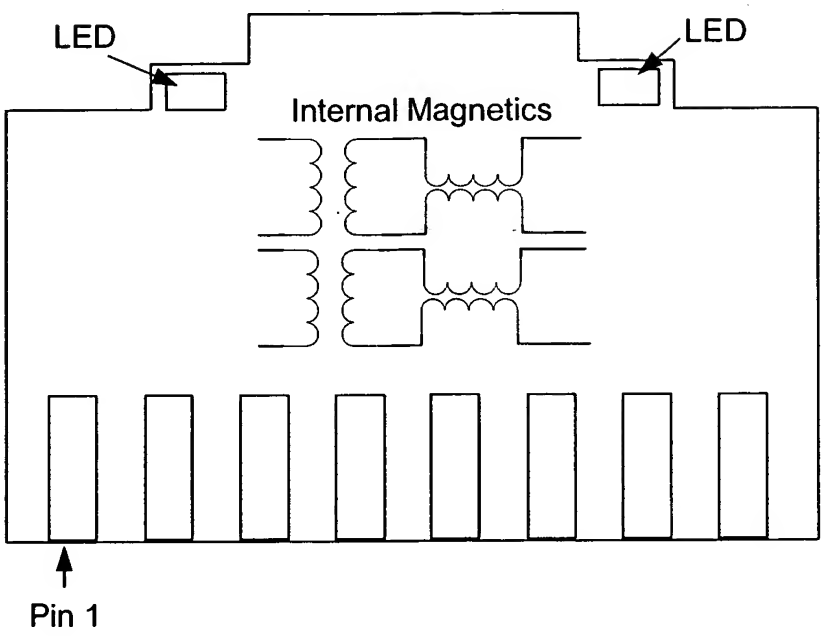

Figure 5-3 Front View of Ethernet RJ-45 Connector

6 POWER REQUIREMENTS

The E35A1 will require the high capacity power supply from the motherboard that is rated at 1.65A at 3.3 volts and 0.5A at 5 volts, & 0.155mA (@ 2V data retention level) from the backup battery on the motherboard. Refer the "Power Estimate for E35A1" spreadsheet for details.

7 TVC (PER PART COST)

Refer the "TVC for E35A1" for the TVC spreadsheet.
Present TVC for the E35A1 is 209$.

8 PHYSICAL AND ENVIRONMENTAL

Parameter	Specification
Size	PCB: 4.84" x 4.75" Module: "5.04 x 4.95"
Shock & Vib.	Testing per Project Design Activity Plan
Reliability	Minimum MTBF defined on Project Design Activity Plan. Deratings applied where necessary to achieve the highest MTBF.
Temperature & Humidity	Operating range of 0 to +60 deg.C at the air inlet to the module with relative humidity between 5% and 95% (Non-Condensing).
EMC Testing	Testing per Project Design Activity Plan. Requirement for the E35A1 to pass CISPR-11 radiated emissions tests outside of a metal enclosure and without conduit.

Table 8-1 Physical and Environmental Specifications

9 SKETCHES

The following is intended to provide a concept view of the appearance of the front faceplate of a CPU374 module. It is not intended to show the final product design or actual product dimensions

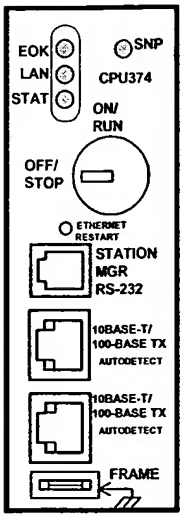

Figure 9-1 Sketch of CPU374

This sketch shows what a CPU374 with 10/100 Ethernet daughterboard might look like from the front. Refer to the existing front label for the CPU364 (44A735985) for comparison and for a basis for the design for the front label for the CPU374. The preliminary mechanical outlines for the E35A1 board is done. The number is 44B714891.